

Model: Florence
Project Code:91.3NG01.001
PCB Ver: 1
PCB Number:13093- -1
PCB P/N:
SCH Ver: 1
PCBA:

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USB2.0 Power SW

USB 3.0 Port

Shark Bay :
Processor : HASWELL(rPGA 946B/947 Socket)
Chipset : LYNX POINT HM86
GPU: nVIDIA N15P-GT-AIO-A1
LAN :RTL8111GA Giga lan
AUDIO :Realtek 269 VC
SIO :ITE 8732F-CX
Card reader :RTS5170
Scalar :RTD2487HTD



For SA modify or change



For SB modify or change



For 1A modify or change



For 1 modify or change

PCB BOARD SIZE

6 Layers

270mmX 180mm

BOM Configuration

Unmount:(R)

Unmount after MP (X)

GPU:(G)

Hynix RAM:(H)

Micron RAM:(M)

UMA: (U)

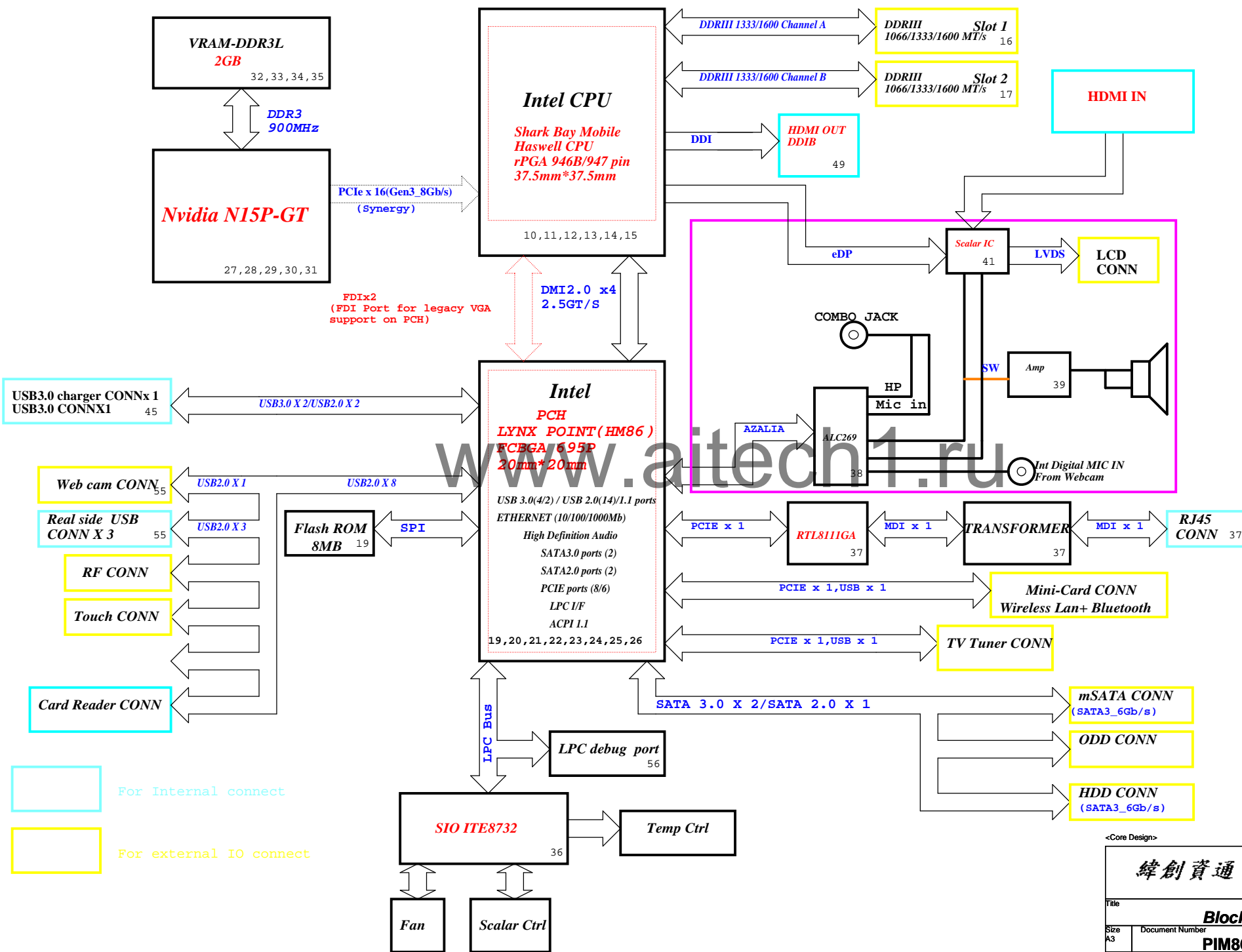
AMP:(A)

SCALAR: (S)

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Florence Block Diagram (GPU)



SYSTEM DC/DC TPS51225		59
INPUTS	OUTPUTS	
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_Charger 3D3V_A	
CPU DC/DC ISL95812HRTZ		63~64
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
SYSTEM DC/DC RT8207LGQW		61
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0	
SYSTEM DC/DC TPS51363		62
INPUTS	OUTPUTS	
DCBATOUT	1D5V_VGA_S0	
LDO APL5930KAI		62
INPUTS	OUTPUTS	
3D3V_S0	1D5V_S0	
SYSTEM DC/DC TPS51116		60
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3 0D675V_S0	
VGA NCP81172		65
INPUTS	OUTPUTS	
DCBATOUT	VGA_CORE	
Switches		66
INPUTS	OUTPUTS	
3D3V_S0	3D3V_VGA_S0	
1D05V_S0	1D05V_VGA_S0	
1D5V_S0	1D5V_VGA_S0	
PCB LAYER		
L1:Top	L5:VCC	
L2:GND	L6:Signal	
L3:Signal	L7:GND	
L4:Signal	L8:Bottom	

SSID = CPU

Table 5-6. Processor PCI Express* Compensation Signal Routing Guidelines

Parameter	Segment	Units	Trace Width	Trace Spacing to Other Signals	Routing Length	Resistance
PEG_RCOMP	L1	mils	12	15	400	NA
Resistor	R1	Ω	NA	NA	NA	24.9 ± 1%

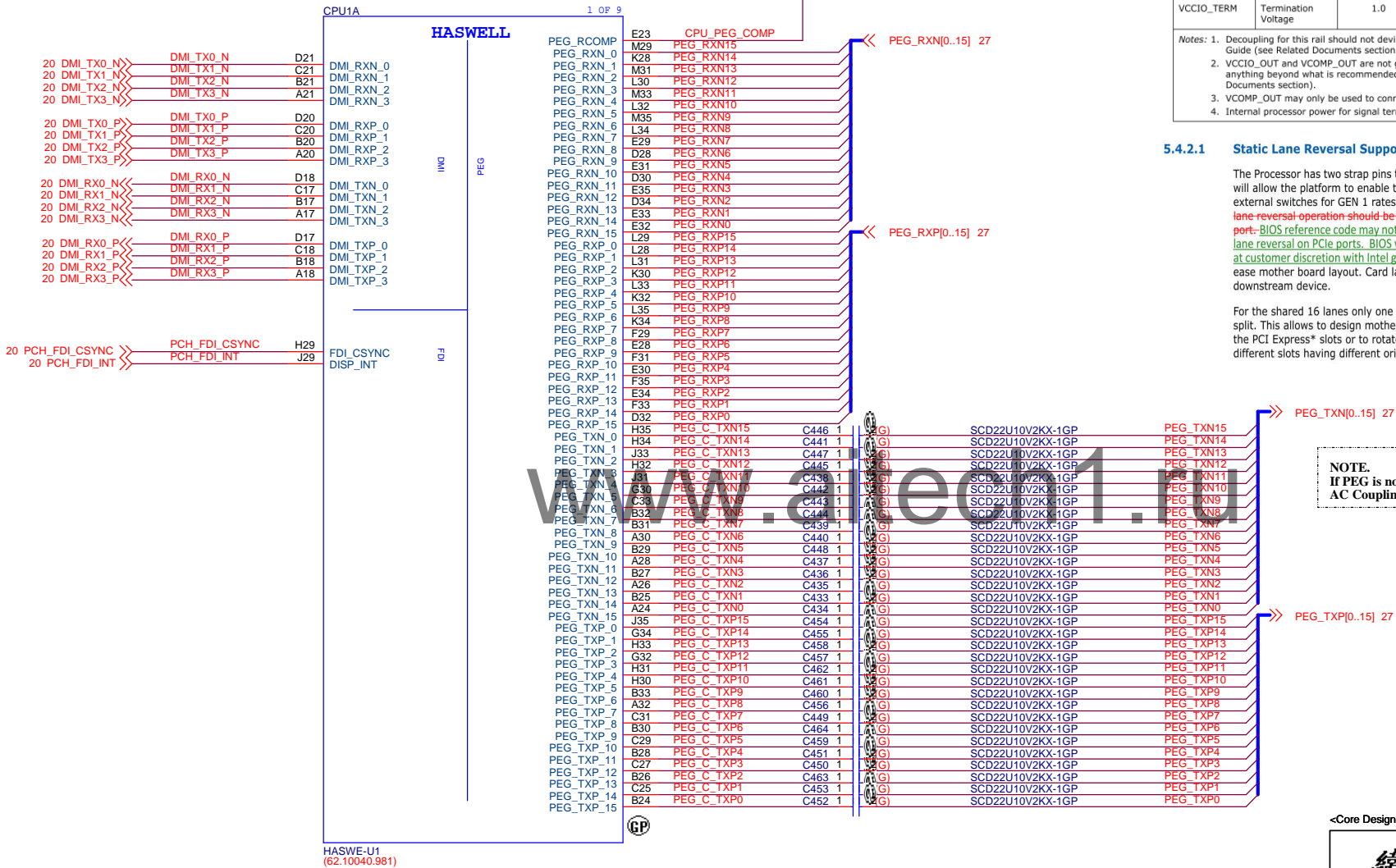


Table 47. VCCIO_OUT, VCOMP_OUT and VCCIO_TERM

Symbol	Parameter	Typ	Max	Units	Notes
VCCIO_OUT	Termination Voltage	1.0		V	1, 2
ICCIO_OUT	Maximum External Load		300	mA	1, 2
VCOMP_OUT	Termination Voltage	1.0		V	1, 2, 3
VCCIO_TERM	Termination Voltage	1.0		V	4

Notes: 1. Decoupling for this rail should not deviate from what is found in the appropriate Platform Design Guide (see Related Documents section).
2. VCCIO_OUT and VCOMP_OUT are not general purpose rails and should not be used to power anything beyond what is recommended in the appropriate Platform Design Guide (see Related Documents section).
3. VCOMP_OUT may only be used to connect to PEG_RCOMP and eDP_RCOMP.
4. Internal processor power for signal termination.

5.4.2.1 Static Lane Reversal Support

The Processor has two strap pins that will be driven by card detect of port B and C. This will allow the platform to enable the second and third controllers and control the external switches for GEN 1 rates. The root port supports static lane reversal. **That is, lane reversal operation should be configured by BIOS before enabling the relevant root port. BIOS reference code may not fully support preset search algorithm on systems with lane reversal on PCIe ports. BIOS will fully support GEN 3 by use of presets programmed at customer discretion with Intel guidance.** The target for the lane reversal support is to ease mother board layout. Card layout is not supported and should be handled by downstream device.

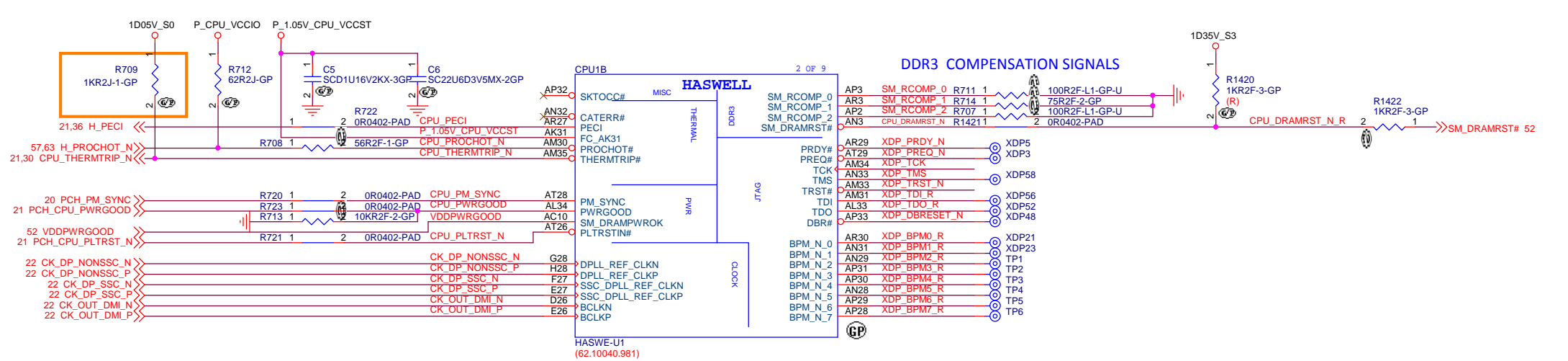
For the shared 16 lanes only one reversal option is supported regardless of the port split. This allows to design motherboard with straight or rotated processor relative to the PCI Express* slots or to rotate all the slots together. There is no support for different slots having different orientation.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect
AC Coupling Cap Value: 180~265 nF

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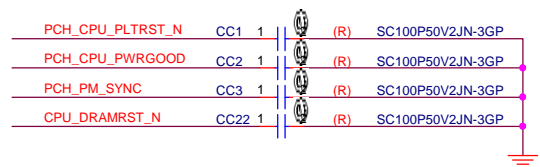
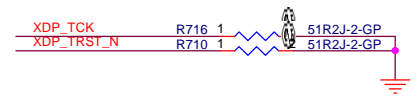
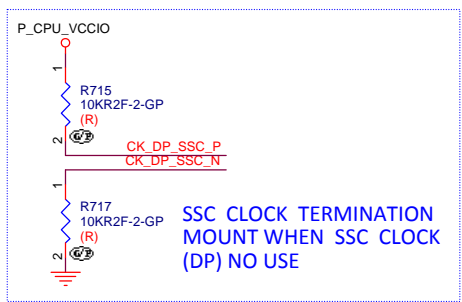
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Title			
CPU (DMI/PCIE)			
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SSID = CPU



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Mount R709 and change to 1K for bring up--Kai 0425



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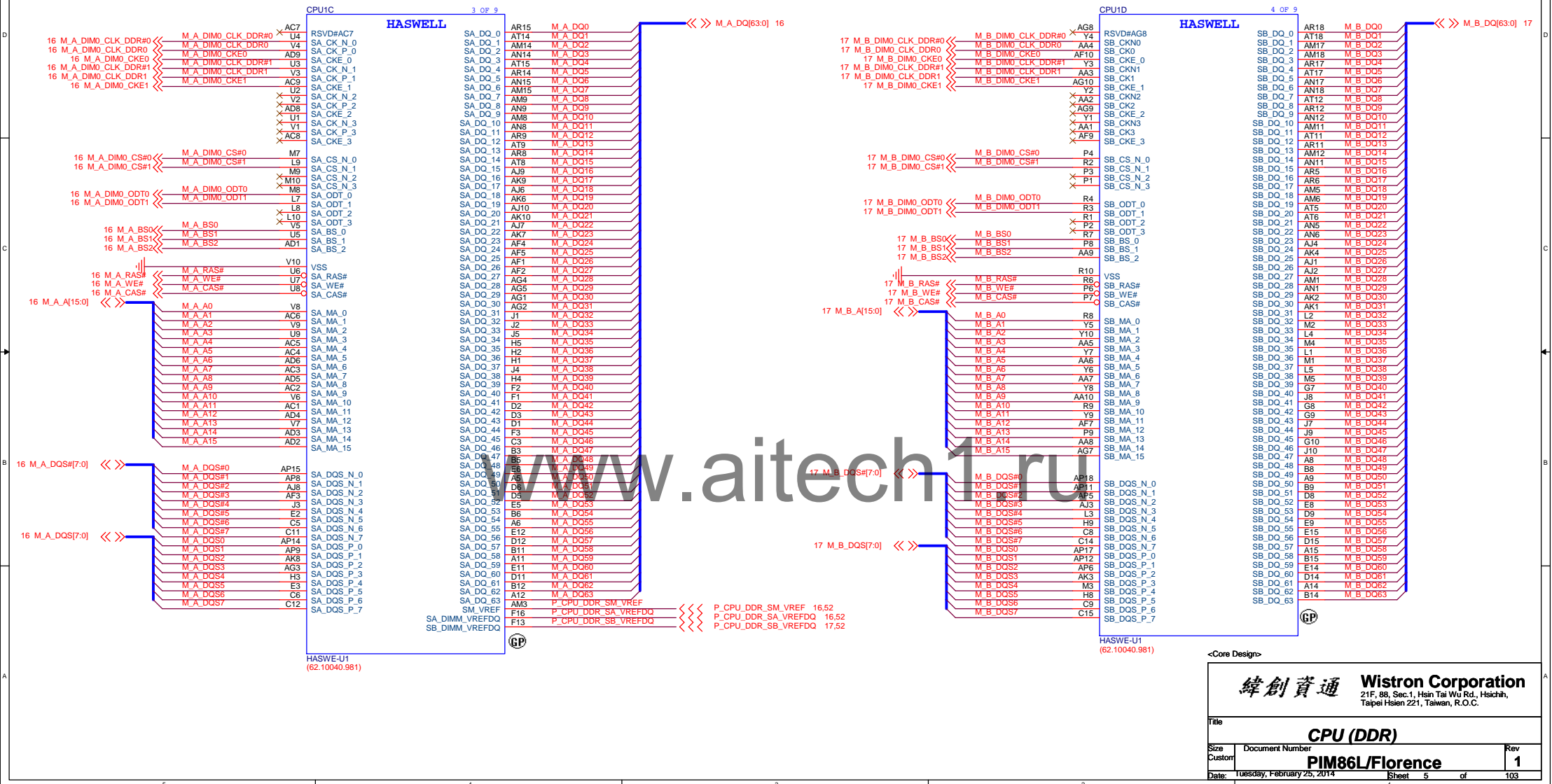
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Title: **CPU (MISC/JTAG/CLK/eDP/FD)**

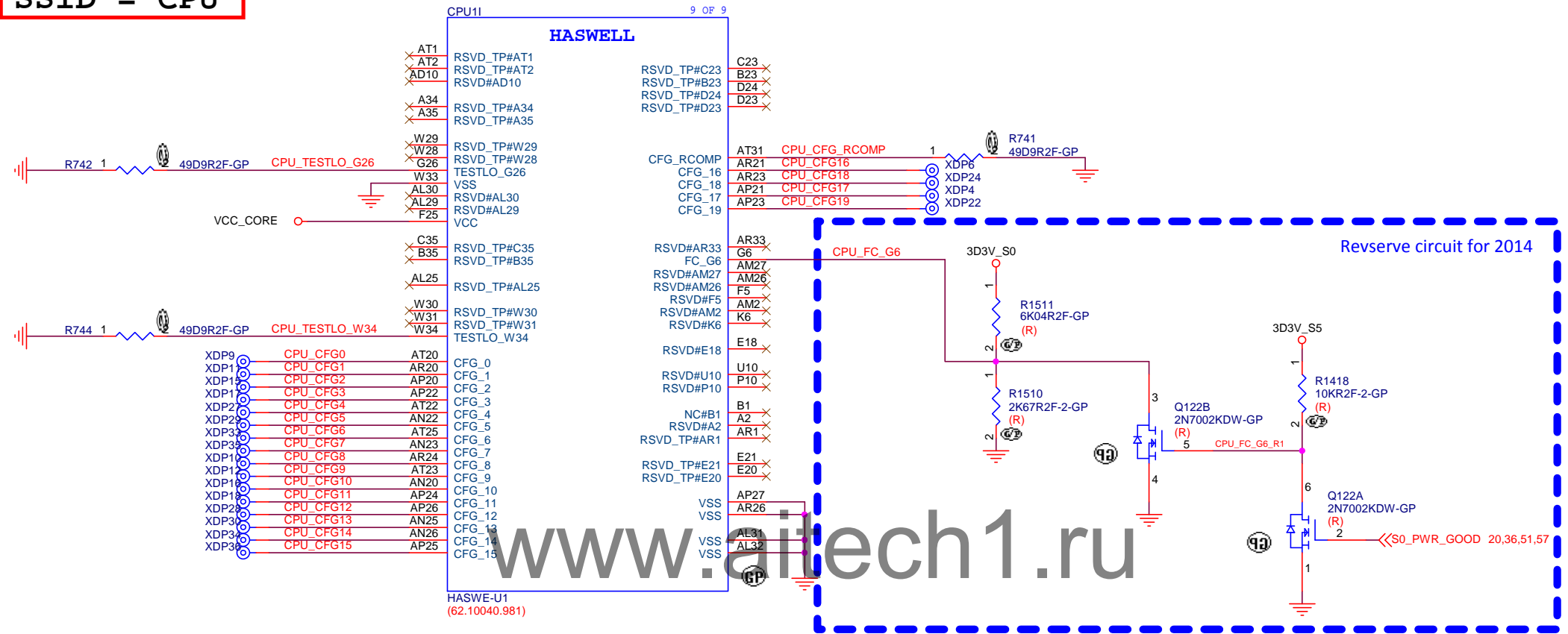
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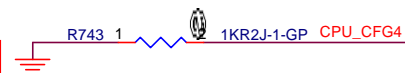
Follow London net name--Kai 0302



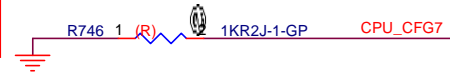
SSID = CPU



Display Port Presence Strap	
CFG4	<p>1: Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0: Enabled; An external Display Port device is connected to the Embedded Display Port</p>



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training



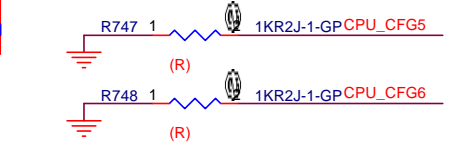
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed



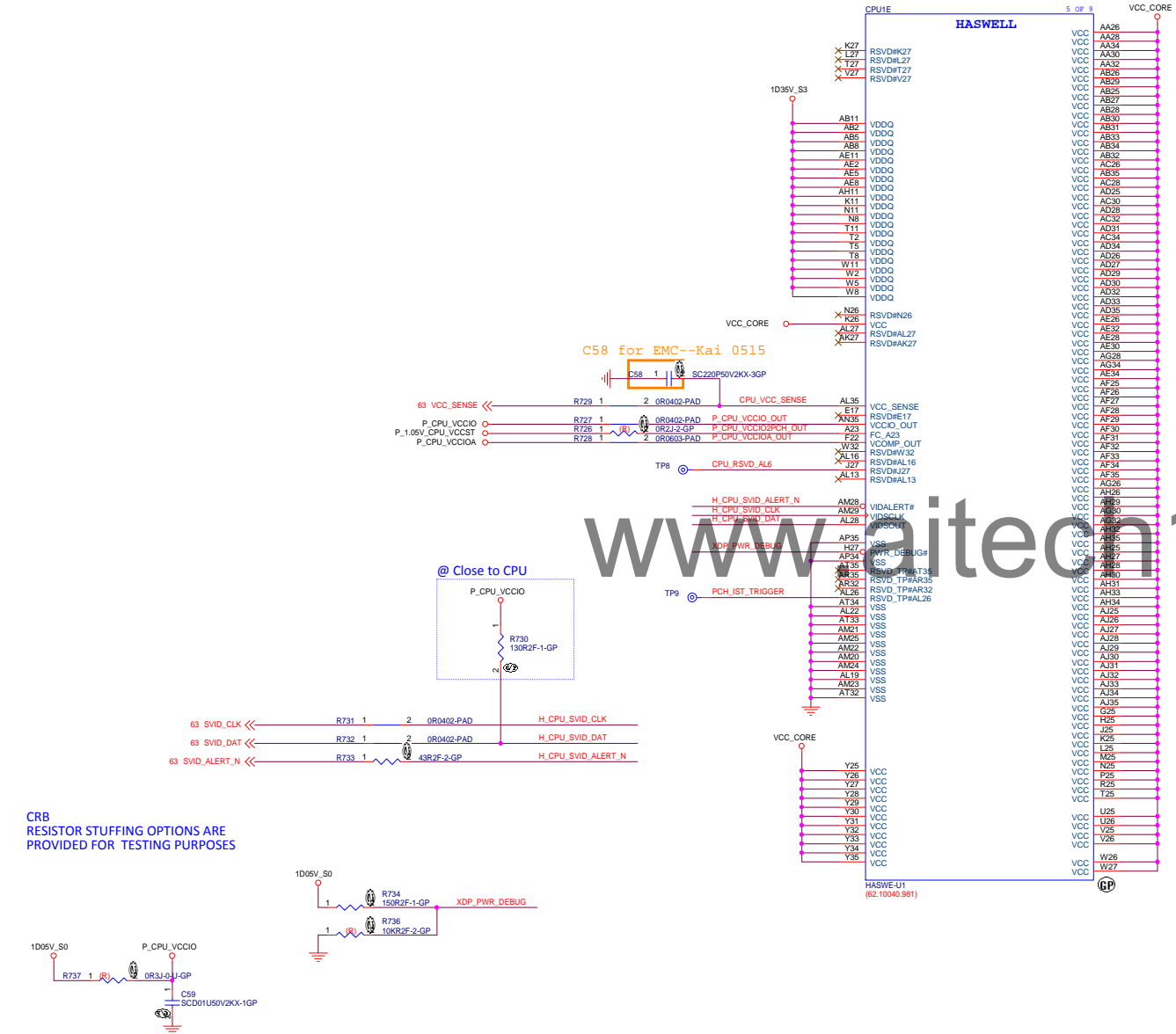
PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG3	0 : ENABLED SET DFX_ENABLED BIT IN DEBUGINTERFACE MSR
	1 : DISABLED



PCIe Port Bifurcation Straps	
CFG[6:5]	11: Device 1 function 1 disabled ; Device 1 function 2 disabled
	10: Device 1 function 1 enabled ; Device 1 function 2 disabled
	01: Device 1 function 1 disabled ; Device 1 function 2 enabled
	00: Device 1 function 1 enabled ; Device 1 function 2 enabled

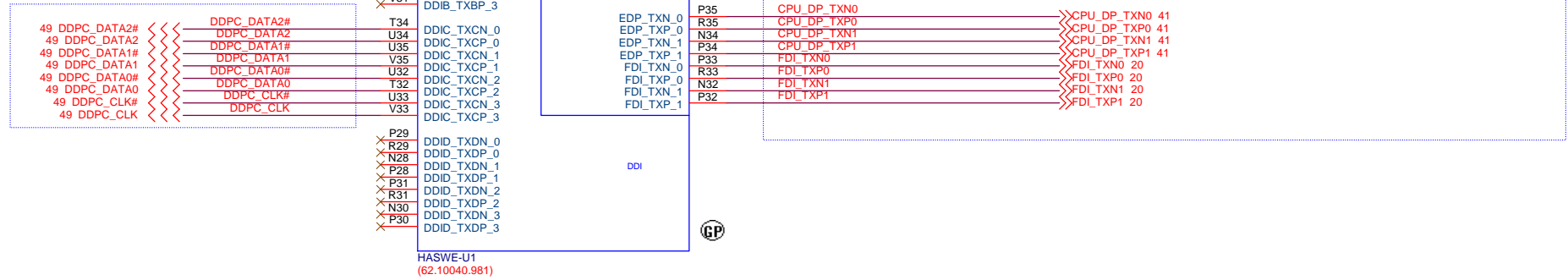


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CRB
RESISTOR STUFFING OPTIONS ARE
PROVIDED FOR TESTING PURPOSES

Note:How to Disable DDI Port? No Connect



- The HDMI* interface supports the HDMI with 3D, 4K, Deep Color, and x.v.Color while the DisplayPort* interface supports the VESA DisplayPort* Standard Version 1, Revision 2.

- In addition, the processor supports a dedicated embedded DisplayPort* (eDPx4) interface. eDPx4 can be configured in one of the following ways:
 - One x2 embedded DisplayPort* and one x2 FDI (FDI Port for legacy VGA support on PCH).
 - FDI_TXN0 and FDI_TXP0 should be routed to EDP_TXN2 and EDP_TXP2, respectively.
 - FDI_TXN1 and FDI_TXP1 should be routed to EDP_TXN3 and EDP_TXP3, respectively.
 - One x4 embedded DisplayPort* and no FDI (no VGA support from PCH in this configuration)Note: One of the two configurations of eDP can be selected using VBIOS Tool (VBT) and hardware gets programmed to function as x4 eDP or x2 eDP and x2 FDI by VBIOS during boot time.

Table 8-1. Configuration-wise Mapping of HDMI signals for Processor on DDI ports

Port	Digital Display Interface Differential Pairs	HDMI Signals	Processor Digital Display Interface Pins
Port B	DPB_LANE0_P	HDMI0_DATA2_P	DDIB_TXP0
	DPB_LANE0_N	HDMI0_DATA2_N	DDIB_TXN0
	DPB_LANE1_P	HDMI0_DATA1_P	DDIB_TXP1
	DPB_LANE1_N	HDMI0_DATA1_N	DDIB_TXBN1
	DPB_LANE2_P	HDMI0_DATA0_P	DDIB_TXBP2
	DPB_LANE2_N	HDMI0_DATA0_N	DDIB_TXBN2
	DPB_LANE3_P	HDMI0_CK_P	DDIB_TXBP3
	DPB_LANE3_N	HDMI0_CK_N	DDIB_TXBN3
	DDPB_HPD	DDSP_1_HPD0	Hot plug detect used by HDMI Port B
	DDPB_CTRLCLK	DPB_CTRL_CK	HDMI DDC lines for Port B
	DDPB_CTRLDATA	DPB_CTRL_DATA	

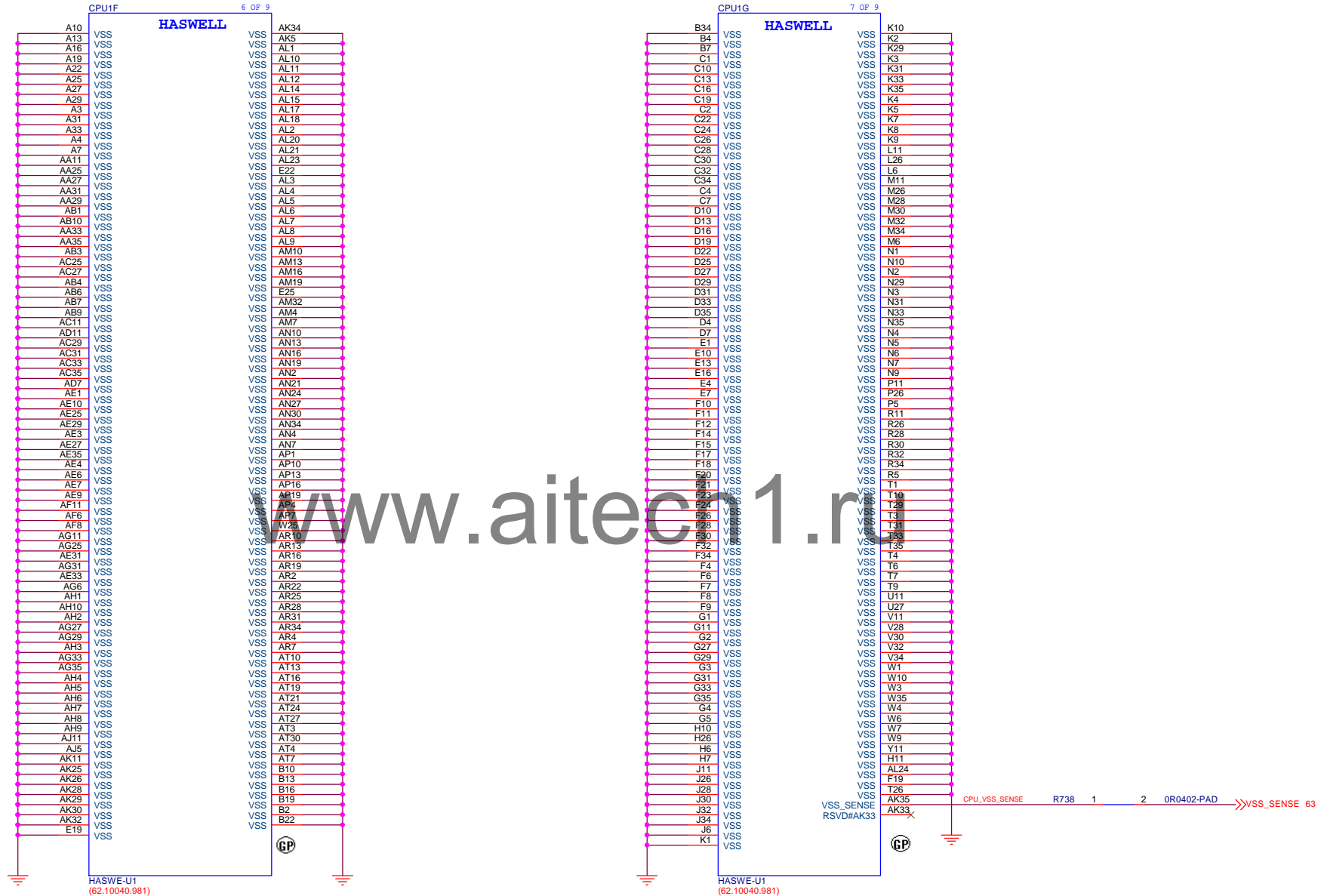
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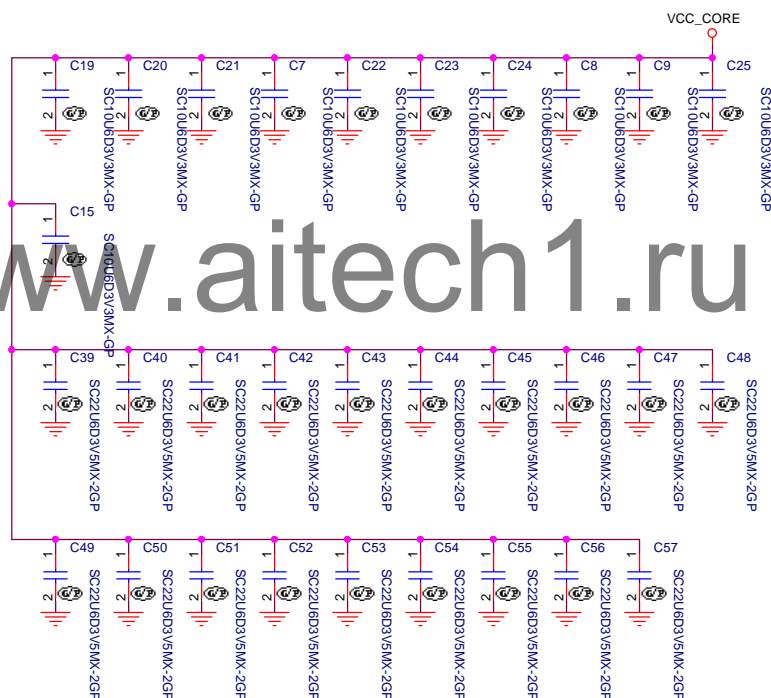
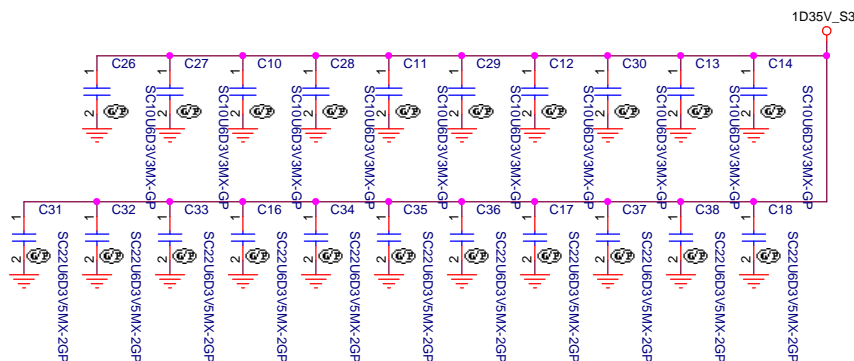
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CPU(DDI/EDP)		
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SSID = CPU



Signal		Value	Quantity	
VCC_CORE	CRB	470uF	5/8	
		22uF	19/19	
		10uF	11/11	
	PPDG	470uF	2	
		22uF	19	
		10uF	11	



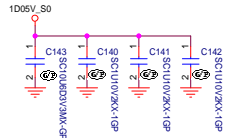
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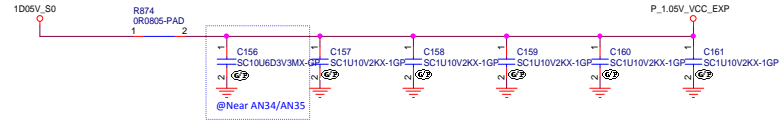
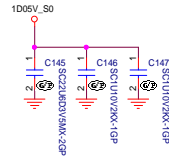
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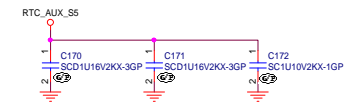
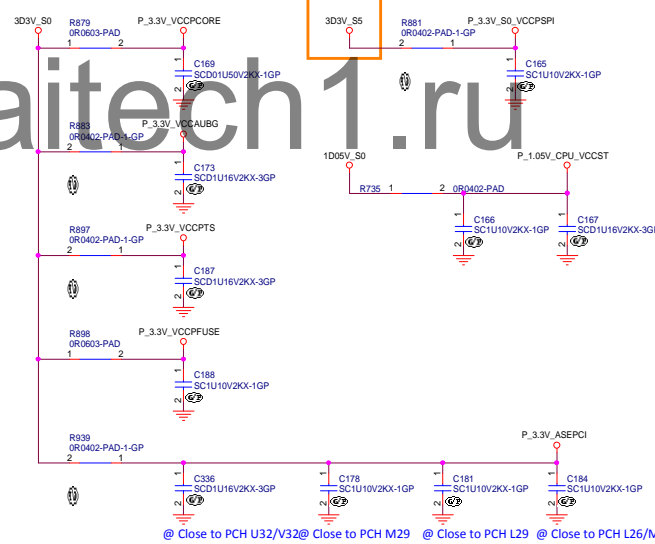
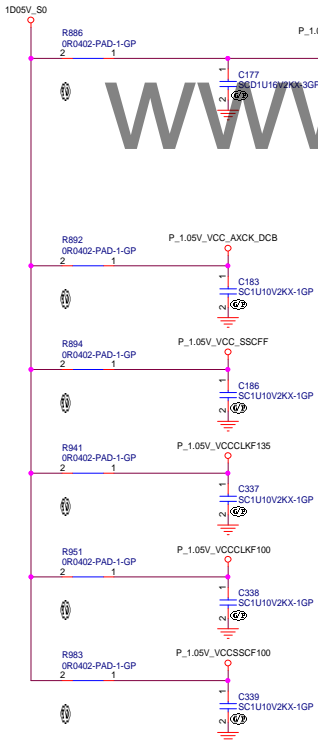
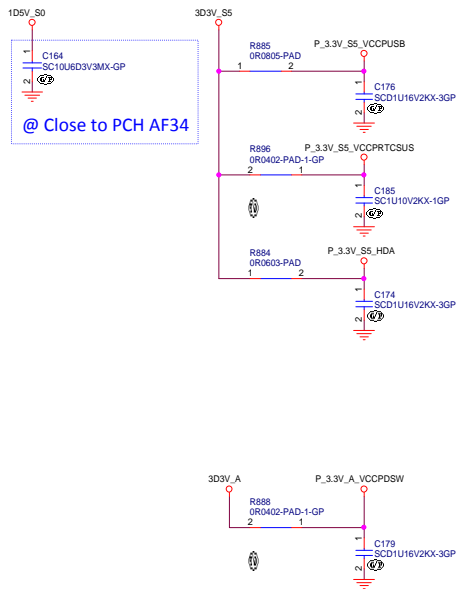
Signal		Value	Quantity	
PCH_VCC	CRB	10uF	1/1	
		1uF	3/3	
	PPDG	10uF	1	
		1uF	3	



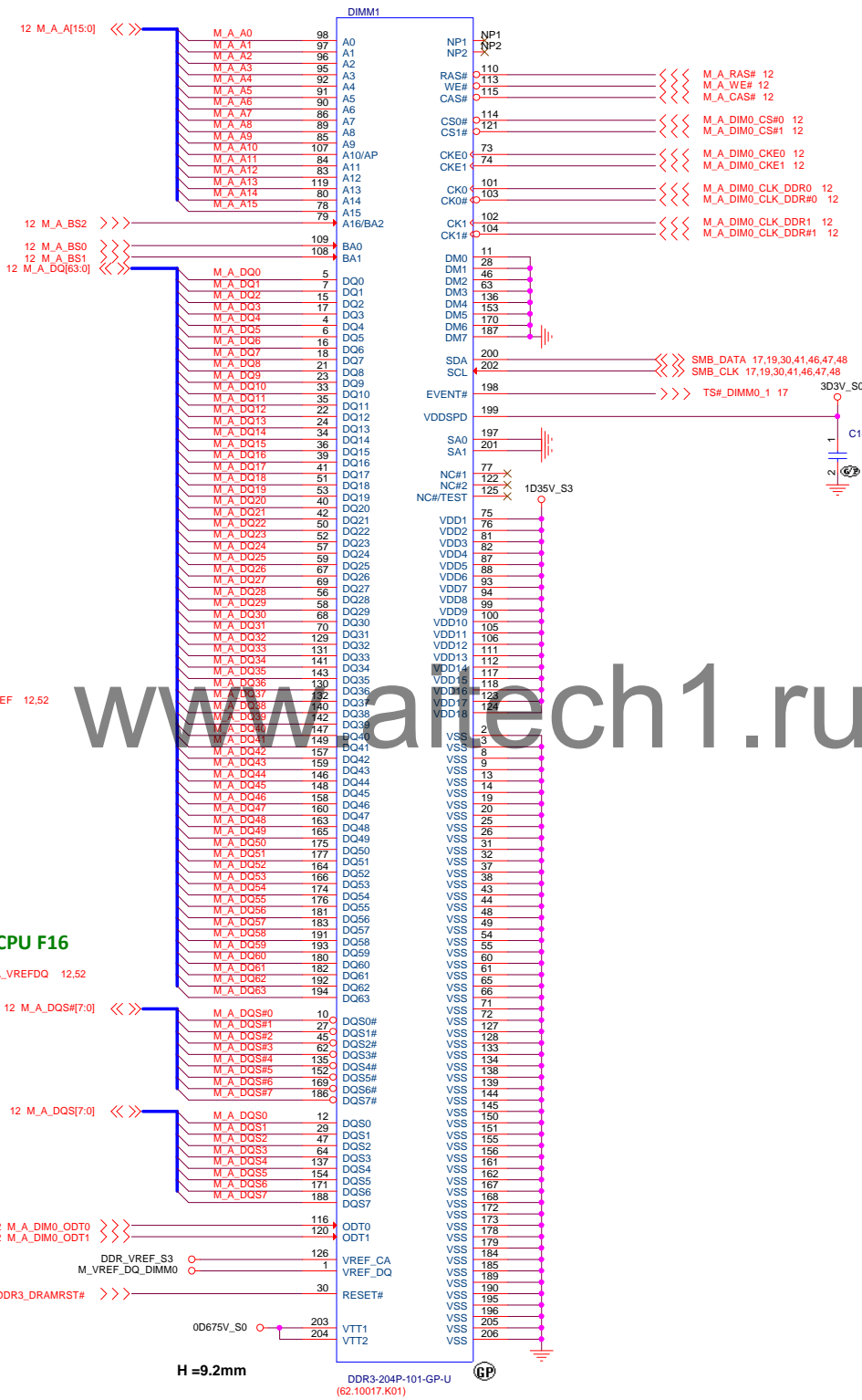
Signal		Value	Quantity	
PCH_VCCASW	CRB	22uF	1/1	
		1uF	2/2	
	PPDG	22uF	1	
		1uF	2	



power from S0 change to S5
power follow SPI power -- Kai
0514

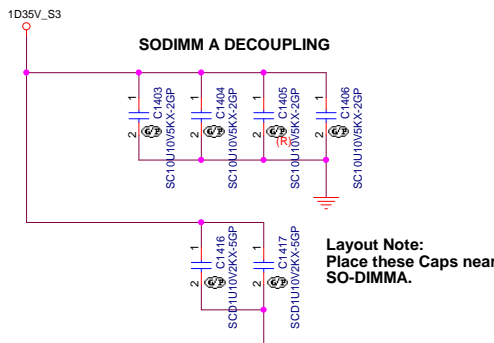
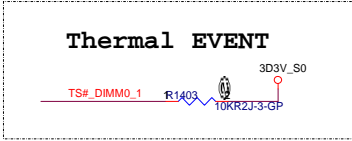


SSID = MEMORY

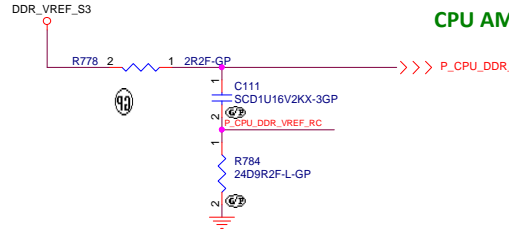


Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

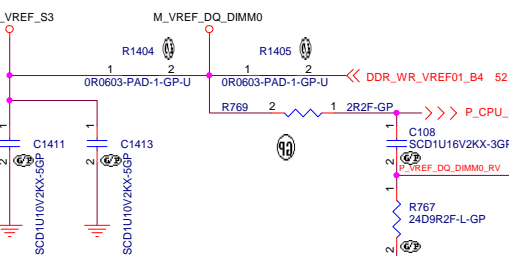


Layout Note:
Place these Caps near
SO-DIMMA.

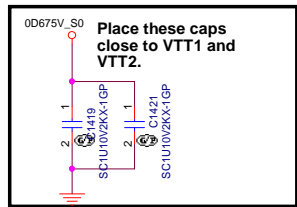


CPU AM3

CPU F16



Tracew should be at least 20 mils wide



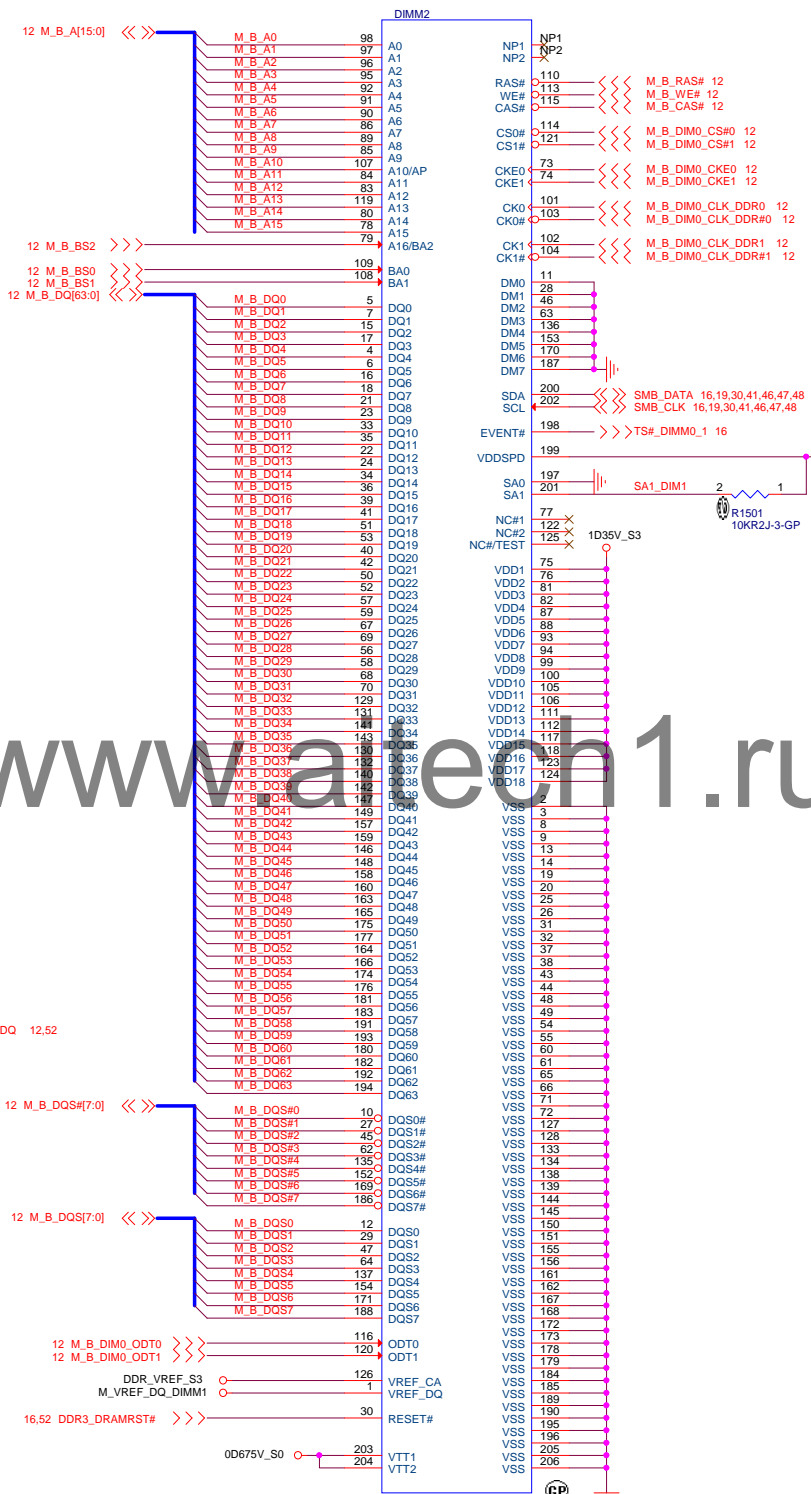
Place these caps
close to VTT1 and
VTT2.

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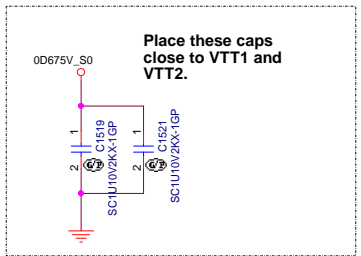
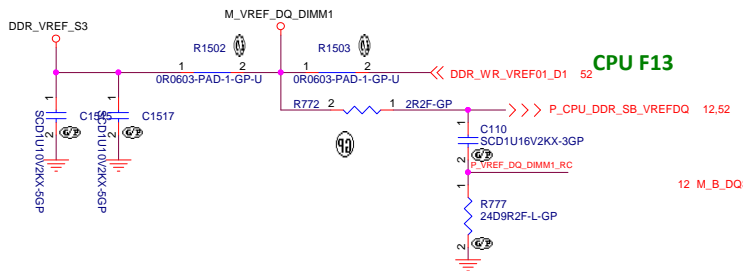
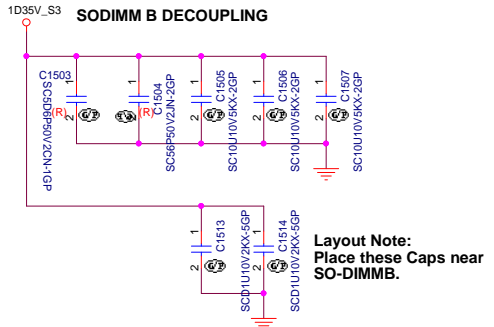
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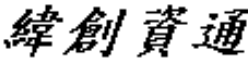
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from
the Processor than SO-DIMMA



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Title DDR3L-SODIMM2			
Size A	Document Number PIM86L-Florence		Rev 1
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SSID = PCH

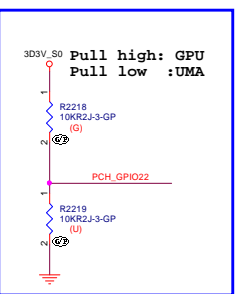
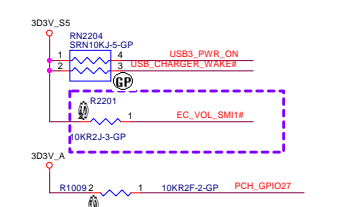
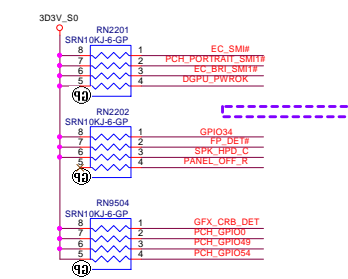
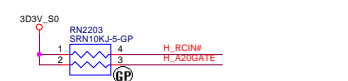
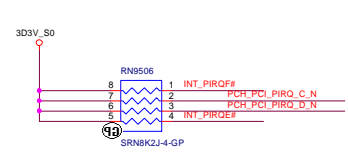
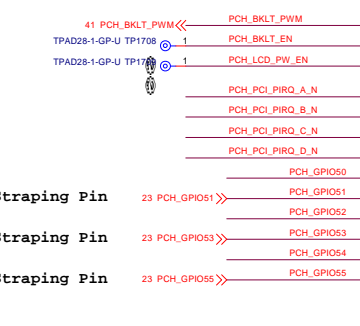


Table 13-15. VGA DAC Disable Recommendations

Signal Name	Recommended Connection
VGA_REG, VGA_GREEN, VGA_BLUE	NC or GND
VGA_BRTN	GND
VGA_HSYNC, VGA_VSYNC	NC
DAC_REFP	GND
DAC_SDA, DAC_DATA	NC
VCCDAC	GND
VCCDACBG	GND



Strapping Pin 23 PCH_GPIO51 >>> PCH_GPIO51
Strapping Pin 23 PCH_GPIO53 >>> PCH_GPIO53
Strapping Pin 23 PCH_GPIO55 >>> PCH_GPIO55

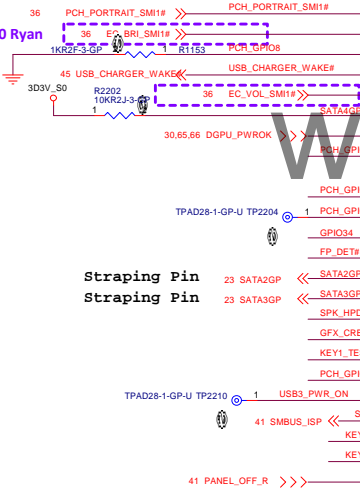
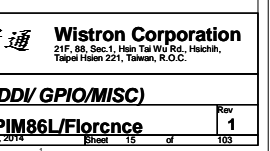
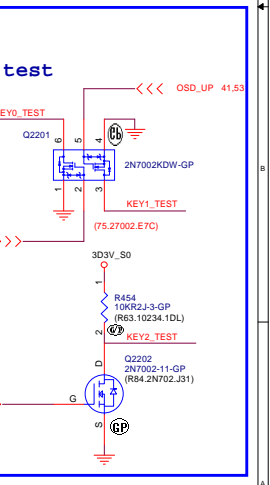
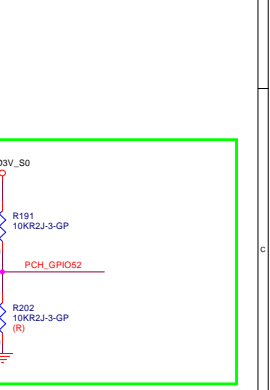
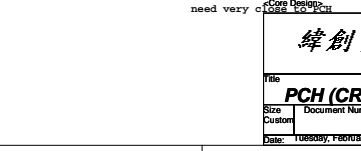
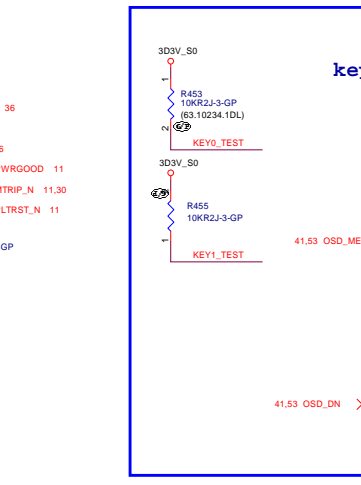
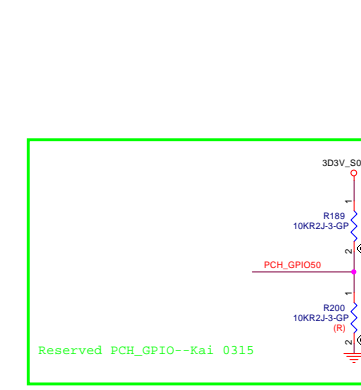
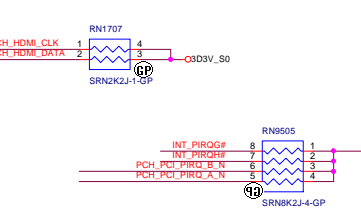
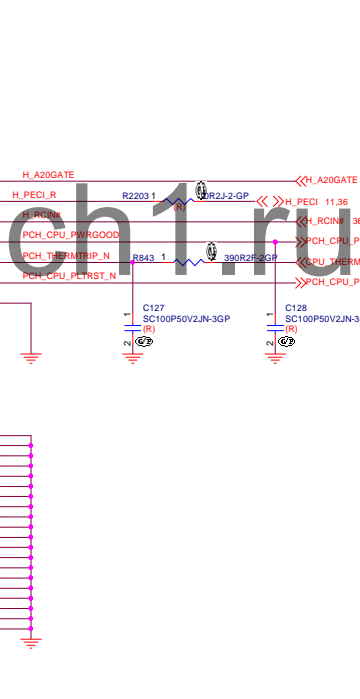
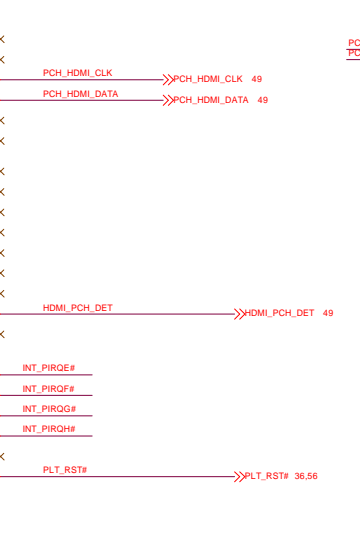
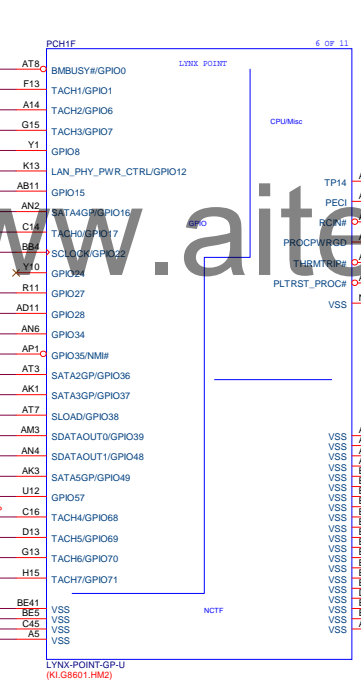
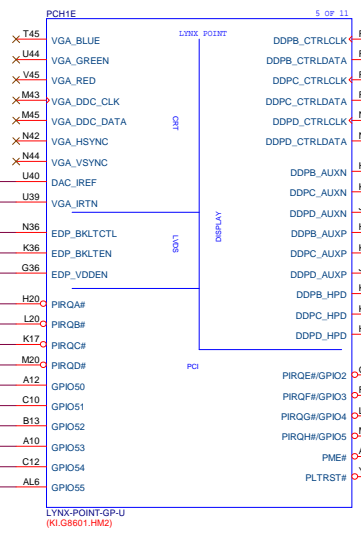


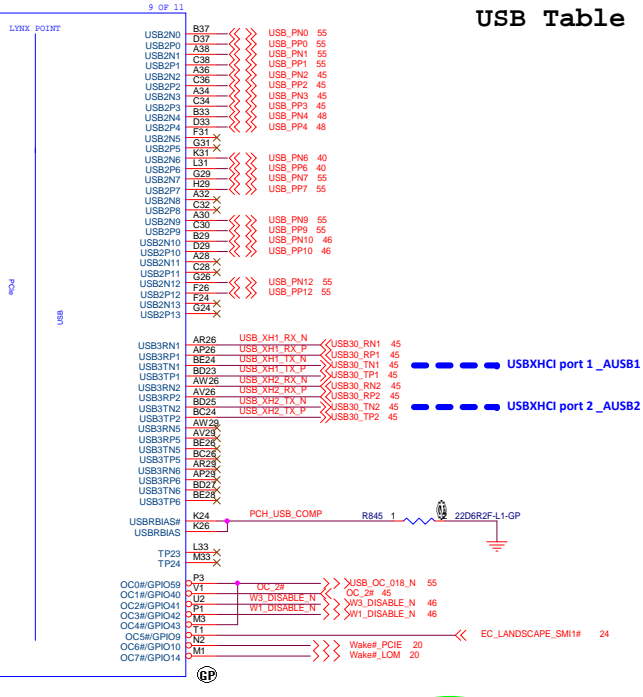
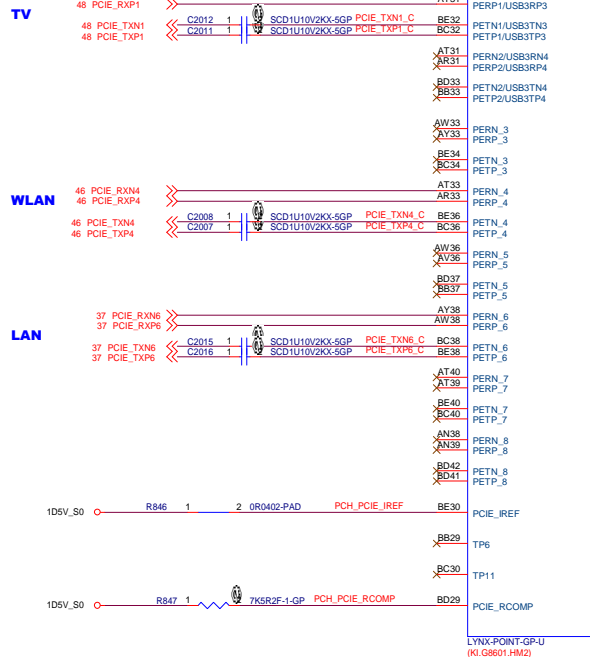
Table 37-4. Enabling Switchable Graphics on Intel Shark Bay RVP

Signal	GPIO Assignment	PEG RSVD Assignments
DGPU_RSMT#	GPIO67	PEG_RSVD3
DGPU_PWR_EN#	GPIO54	PEG_RSVD5
DGPU_PWROK	GPIO17	PEG_RSVD2
DGPU_HOLD_RST#	GPIO50	N/A*
DGPU_HRD_INTR#	GPIO6	PEG_RSVD6

Note: * DGPU_HOLD_RST# is routed to the PWROK pin on the PCIe x16 connector.



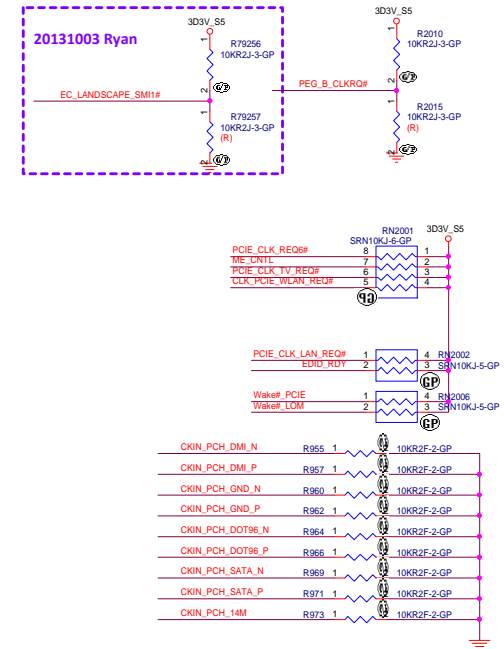
SSID = PCH



USB Table

Pair	Device
0	Ext. USB2.0
1	Ext. USB2.0
2	USB3.0 Ext. port 0
3	USB3.0 Ext. port 1
4	TV Tuner
5	X
6	CR
7	Touch
8	X
9	Ext. USB2.0
10	Bluetooth
11	Dongle
12	Webcam
13	X

SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
QM87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 6	USB 3.0 Port 5 PCi* Port 1	USB 3.0 Port 4 PCi* Port 2	PCi* Port 3	PCi* Port 4	PCi* Port 5	PCi* Port 6	PCi* Port 7	PCi* Port 8	SATA 6Gbps Port 1	SATA 6Gbps Port 2	SATA 6Gbps Port 3	SATA 3Gbps Port 1	SATA 3Gbps Port 2	SATA 3Gbps Port 3
HM87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 6	USB 3.0 Port 5 PCi* Port 1	USB 3.0 Port 4 PCi* Port 2	PCi* Port 3	PCi* Port 4	PCi* Port 5	PCi* Port 6	PCi* Port 7	PCi* Port 8	SATA 6Gbps Port 1	SATA 6Gbps Port 2	SATA 6Gbps Port 3	SATA 3Gbps Port 1	SATA 3Gbps Port 2	SATA 3Gbps Port 3
HM86	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	USB 3.0 Port 5 PCi* Port 1	USB 3.0 Port 4 PCi* Port 2	PCi* Port 3	PCi* Port 4	PCi* Port 5	PCi* Port 6	PCi* Port 7	PCi* Port 8	SATA 6Gbps Port 1	SATA 6Gbps Port 2	SATA 3Gbps Port 1	NA	SATA 3Gbps Port 2	NA



<Core Design>

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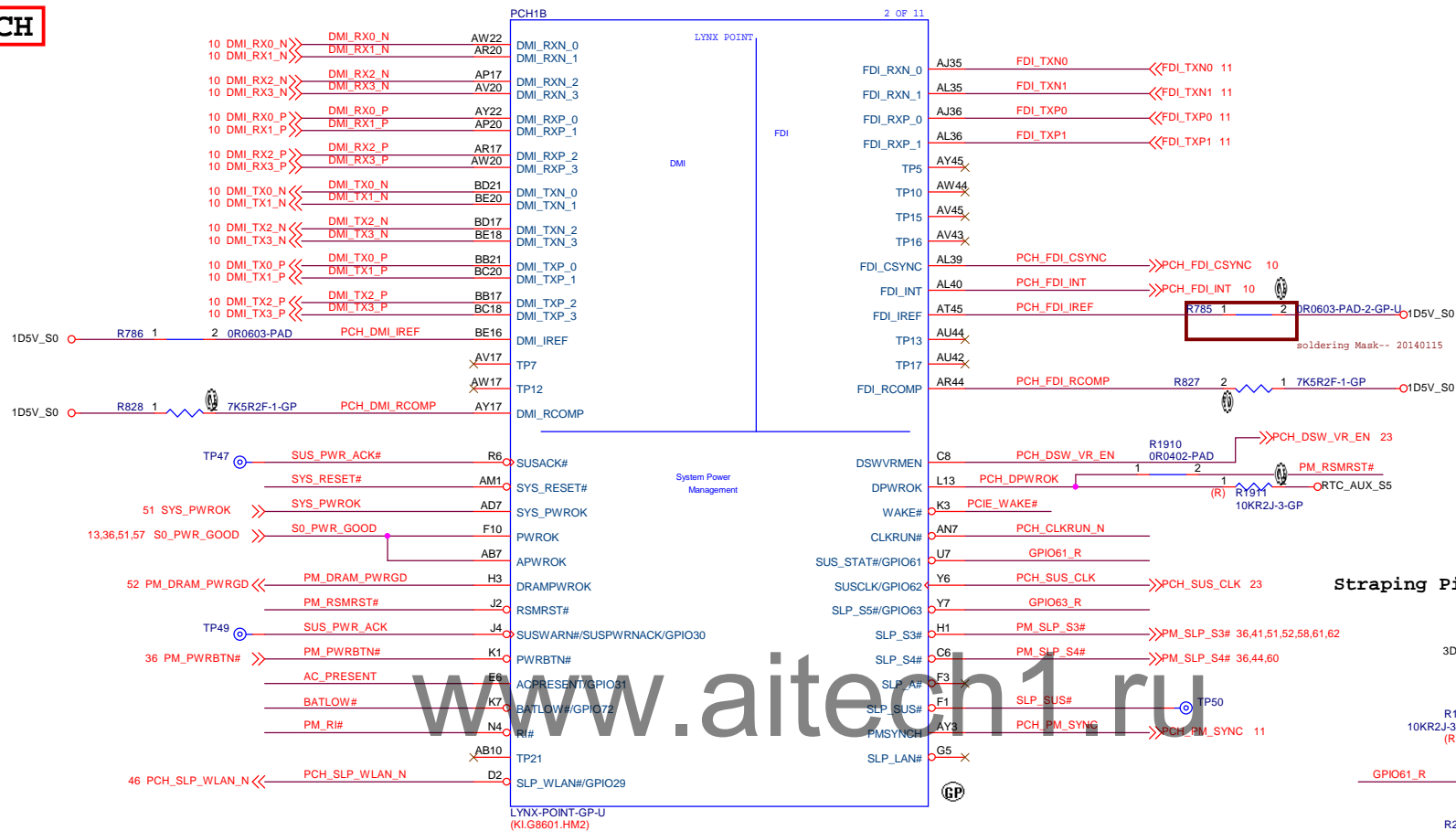
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (PCIE/USB/CLK)
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Size C	Document Number PIM86L/Florence
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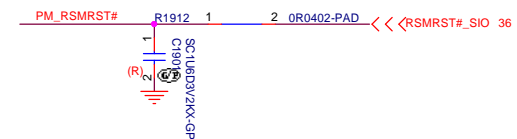
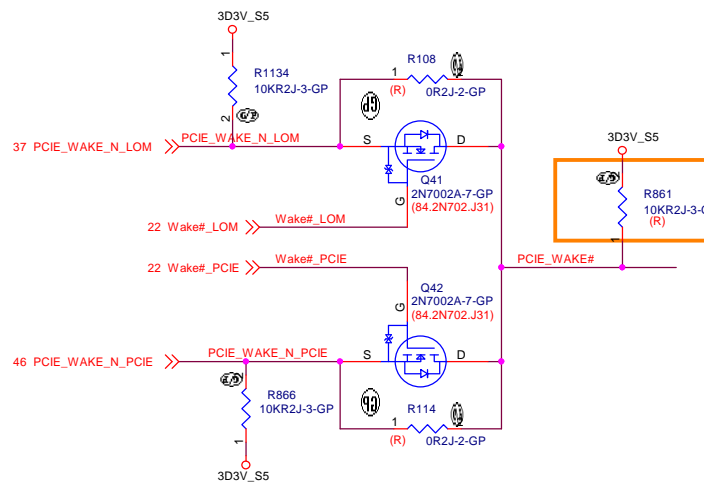
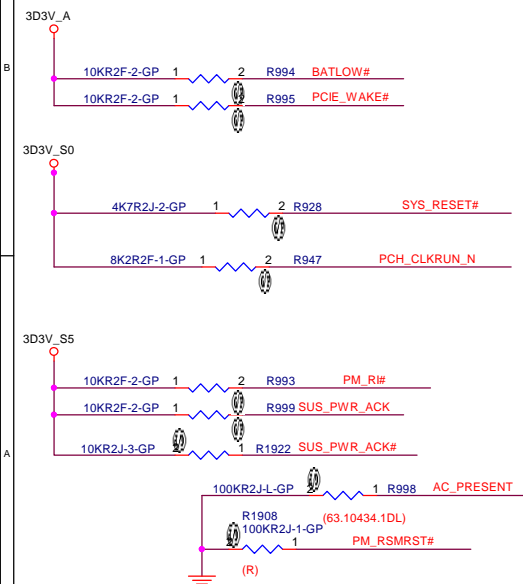
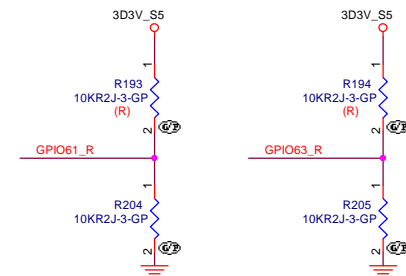
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SSID = PCH

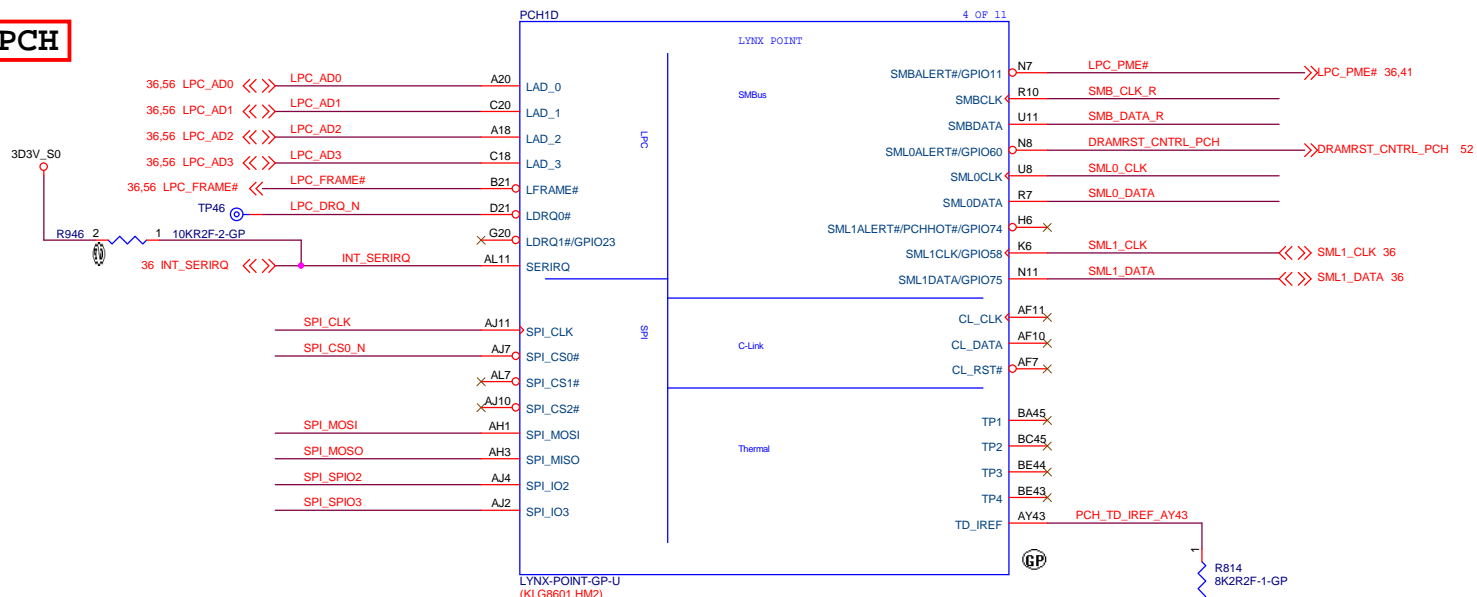


Straping Pin

Straping Pin

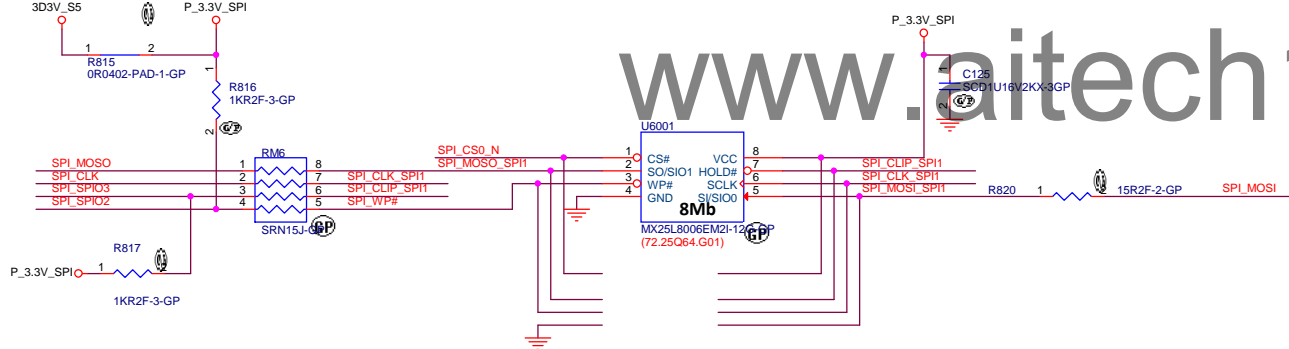


SSID = PCH



SYSTEM SPI ROM

SPI ROM Equal length need to less than 500mil



22.3.1.1 SPI Single Flash Device Routing Guideline

Figure 22-2. SPI Single Flash Device Routing Guidelines for MISO, MOSI and CLK

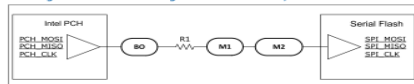


Figure 22-3. SPI Single Flash Device Routing Guidelines for I/O2 and I/O3

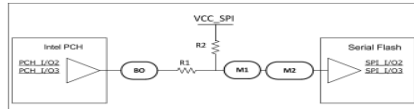
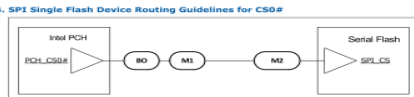


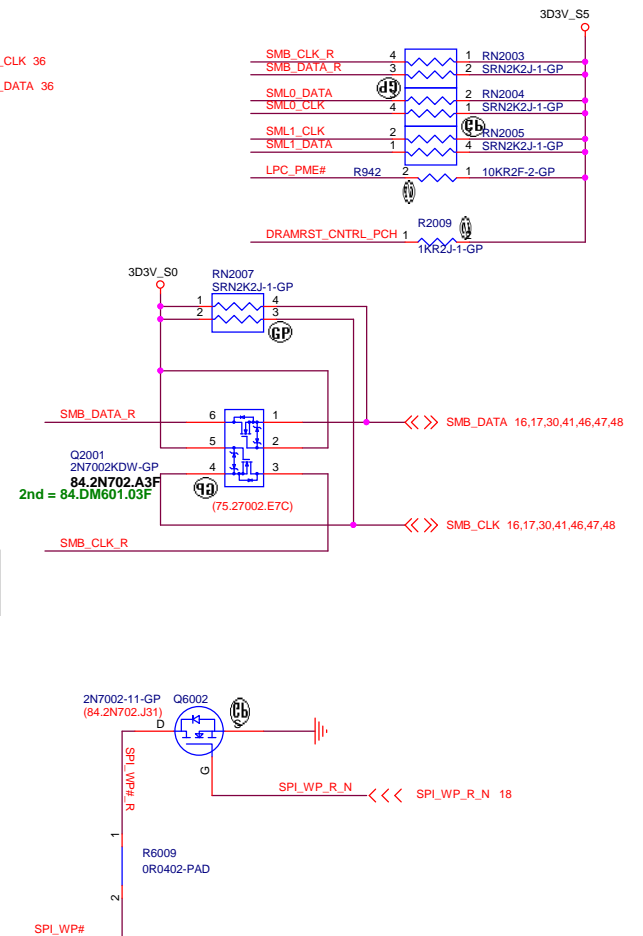
Figure 22-4. SPI Single Flash Device Routing Guidelines for CS0#



4M SPI ROM
72.25Q32.E01 WINBOND W25Q32BVSSIG
1M SPI ROM
72.25Q80.001 WINBOND W25Q80BVSSIG

Table 22-3. SPI Single Flash Device Routing Guidelines (Sheet 2 of 2)

Parameter	Segment	Stackup	Unit	Routing Recommendation
Breakout Trace Length	BO	MS,SL	inch	<1"
Length 1	M1	MS,SL	inch	1"-5"
Length 2	M2	MS,SL	inch	0.5"-1"
Total length	BO, M1, M2	MS,SL	inch	1.5" - 7"
Resistor	R1		ohm	15
Resistor	R2		ohm	1k



<Core Design>

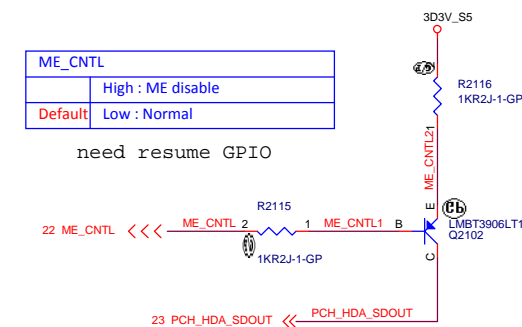
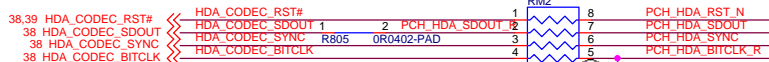
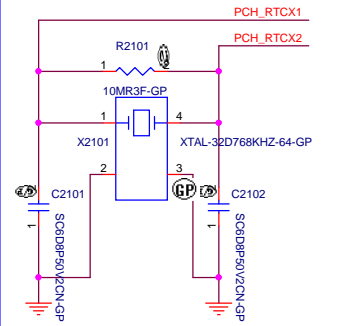
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (LPC/SPI/SMB/THERM)**
Size: Custom Document Number: **PIM86L/Florence** Rev: **1**
Date: Tuesday, February 26, 2014 Sheet: 18 of 103

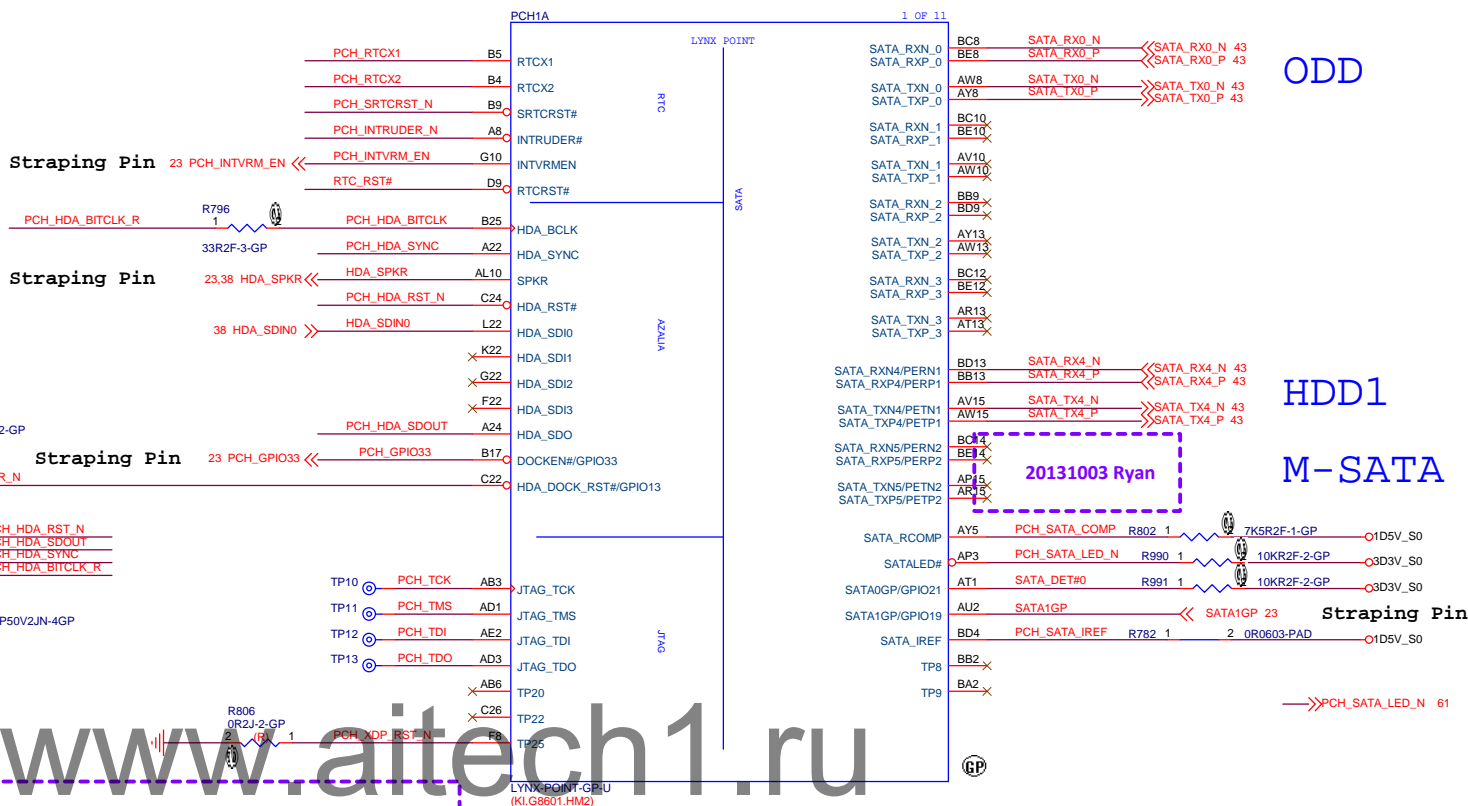
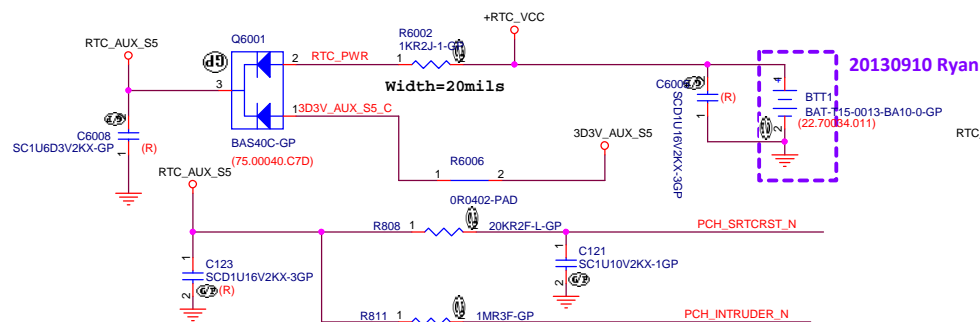
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RTC CRYSTAL

Follow London --Kai 0302



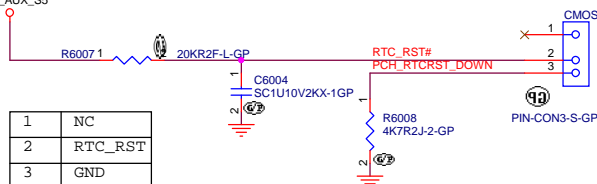
CMOS Circuit



SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
QM87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 PCIe* Port 1	USB 3.0 Port 4 PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 PCIe* Port 1	SATA 6Gb/s Port 5 PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 3Gb/s Port 2	SATA 3Gb/s Port 3
HM87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 PCIe* Port 1	USB 3.0 Port 4 PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 PCIe* Port 1	SATA 6Gb/s Port 5 PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 3Gb/s Port 2	SATA 3Gb/s Port 3
HM86	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	USB 3.0 Port 3 PCIe* Port 1	USB 3.0 Port 4 PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4	SATA 6Gb/s Port 5	SATA 3Gb/s Port 0	NA	SATA 3Gb/s Port 2	NA

Clear CMOS

1	NC
2	RTC_RST
3	GND



<Core Design>

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

PCH (RTC/AUDIO/SATA/JTAG)

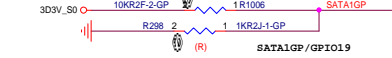
Size Custom	Document Number PIM86L/Florence	Rev 1
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Date: Monday, March 03, 2014 Sheet 19 of 103

SSID = PCH

STRAP

18 SATA1GP
21 PCH_GPIO51
21 SATA1GP
21 SATA3GP
18 PCH_HDA_SDOOUT
18 PCH_GPIO33
18 PCH_INTVRM_EN
20 PCH_SUS_CLK
20 PCH_DSW_VR_EN
18,38 HDA_SPKR
21 PCH_GPIO33
21 PCH_GPIO55



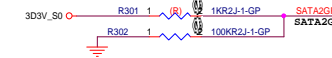
BOOT SELECT STRAPS

BOOT DEVICE	GNT1/ GPIO51	SATA1GP /GPIO19
LPC	0	0
SPI	1	1

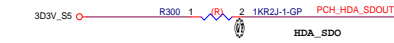
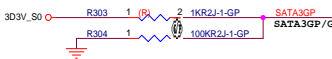
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WEAK INTERNAL PULLUPS ON GP51. DEFAULT SPI BOOT DEVICE.



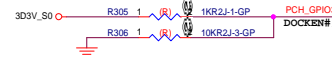
DESIGN NOTE:
DMI RX TERMINATION



DESIGN NOTE:
LOW:TLS CIPHER SUITE WITH NO CONFIDENTIALITY.
HIGH:TLS CIPHER SUITE WITH CONFIDENTIALITY.



DESIGN NOTE:
DMI TX TERMINATION



Straping Pin define

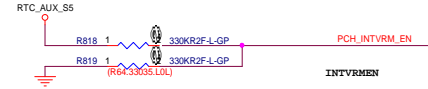
Table 2-17. Functional Strap Definitions (Sheet 1 of 6)

Signal	Usage	When Sampled	Comment															
			This signal has a weak internal pull-up.															
			This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap.															
			<table><tr><th>Bit11</th><th>Bit 10</th><th>Boot BIOS Destination</th></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>Reserved</td></tr><tr><td>1</td><td>1</td><td>SPI (default)</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	Reserved	1	1	SPI (default)	0	0	LPC
Bit11	Bit 10	Boot BIOS Destination																
0	1	Reserved																
1	0	Reserved																
1	1	SPI (default)																
0	0	LPC																
SATA1GP / GPIO19	Boot BIOS Strap bit 0 (BB50)	Rising edge of PWROK	<p>NOTES:</p> <ol style="list-style-type: none">The internal pull-up is disabled after PLTRST# deasserts.If option 00 (LPC) is selected, BIOS may still be placed on LPC, but the platform is required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN.See Chapter 10, "GCS—General Control and Status Register" for additional information.This signal is in the Core well.															

Signal	Usage	When Sampled	Comment															
			<p>This signal has a weak internal pull-up.</p> <p>This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.</p> <table><tr><th>Bit11</th><th>Bit 10</th><th>Boot BIOS Destination</th></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>Reserved</td></tr><tr><td>1</td><td>1</td><td>SPI (default)</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table> <p>NOTES:</p> <ol style="list-style-type: none">The internal pull-up is disabled after PLTRST# deasserts.If option 00 (LPC) is selected, BIOS may still be placed on LPC, but the platform is required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN.See Chapter 10, "GCS—General Control and Status Register" for additional information.This signal is in the Core well.	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	Reserved	1	1	SPI (default)	0	0	LPC
Bit11	Bit 10	Boot BIOS Destination																
0	1	Reserved																
1	0	Reserved																
1	1	SPI (default)																
0	0	LPC																
GPIO51	Boot BIOS Strap bit 1 (BB51)	Rising edge of PWROK	<p>This signal has a weak internal pull-up.</p> <p>This signal only takes effect if DMI is configured in AC-coupled mode (server/workstation only).</p> <p>0 = DMI RX is terminated to VSS. 1 = DMI RX is terminated to VCC/2.</p> <p>NOTES:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# deasserts.If DMI is operating in AC-coupled mode (e.g. client applications), then DMI RX is terminated to VSS and the value of this strap is ignored by the BIOS and the operating system.This signal is in the Core well.															
SATA2GP / GPIO36	DMI RX Termination	Rising edge of PWROK																

Table 2-17. Functional Strap Definitions (Sheet 3 of 6)

Signal	Usage	When Sampled	Comment
SATA3GP / GPIO37	TLS Confidentiality	Rising edge of PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.</p> <p>NOTES:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# deasserts.This signal is in the Core well.
HDA_SDO	Flash Descriptor Security Override	Rising edge of PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Enable security measures defined in the Flash Descriptor. 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.</p> <p>NOTES:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# deasserts.Asserting HDA_SDO high on the rising edge of PWROK will also halt Intel® Management Engine after chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.This signal is in the Suspend well.
HDA_DOCK_EN# / GPIO33	DMI TX Termination	Rising edge of PWROK	<p>This signal has a weak internal pull-down.</p> <p>This signal only takes effect if DMI is configured in DC-coupled mode.</p> <p>0 = DMI TX is terminated to VSS. 1 = DMI TX is terminated to VCC/2.</p> <p>NOTES:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# deasserts.If DMI is operating in AC-coupled mode, then DMI TX is terminated to VCC/2 and the value of this strap does not take effect.This signal is in the Core well.



DSWODVREN - On Die DSW VR Enable	Enabled (DEFAULT)
HIGH	Enabled (DEFAULT)
LOW	Disabled

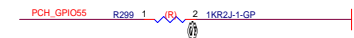
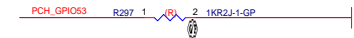


Table 2-17. Functional Strap Definitions (Sheet 4 of 6)

Signal	Usage	When Sampled	Comment
INTVRMEN	Integrated VRM Enable	Always	<p>This signal does not have an internal resistor; an external resistor is required.</p> <p>0 = DCPUS1, DCPUS2 and DCPUS3 are powered from an external power source (should be connected to an external VDD). External VR power is not for Mobile Only; Desktop/Server/Workstation should not pull the strap low. 1 = Integrated VRMs enabled. DCPUS1, DCPUS2 and DCPUS3 can be left as No Connect.</p> <p>NOTES:</p> <ol style="list-style-type: none">This signal is always sampled.This signal is in the RTC well.
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	Rising edge of RSMRST#	<p>This signal has a weak internal pull-up.</p> <p>0 = Disable PLL On-Die voltage regulator. 1 = Enable PLL On-Die voltage regulator.</p> <p>NOTES:</p> <ol style="list-style-type: none">The internal pull-up is disabled after RSMRST# deasserts.This signal is in the Suspend well.
DSWVRMEN	DeepSx Well On-Die Voltage Regulator Enable	Always	<p>This signal does not have an internal resistor; an external resistor is required.</p> <p>0 = Disable Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only supported for testing environments. 1 = Enable DSW 3.3V-to-1.05V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards.</p> <p>NOTES:</p> <ol style="list-style-type: none">This signal is always sampled.This signal is in the RTC well.
SPKR	No Reboot	Rising edge of PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = Disable "No Reboot" mode (PCH will disable the TCO Timer option reboot feature). This function is useful when running ITP/ADP.</p> <p>NOTES:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# deasserts.The status of this strap is readable using the NO REBOOT bit (Chipset Config Registers: RCBA + Offset 3410h:Bit 3).See Chapter 10, "GCS—General Control and Status Register" for additional information.This signal is in the Core well.

Table 2-17. Functional Strap Definitions (Sheet 5 of 6)

Signal	Usage	When Sampled	Comment
GPIO53	DMI AC-Coupling or DC-Coupling Mode	Rising edge of PWROK	<p>This signal has a weak internal pull-up.</p> <p>0 = DMI is in AC-coupling mode (server/workstation only, not meant for desktop/mobile). 1 = DMI is in DC-coupling mode (desktop, mobile or server/workstation).</p> <p>NOTES:</p> <ol style="list-style-type: none">The internal pull-up is disabled after PLTRST# deasserts.This signal is in the Core well.
GPIO55	Top Swap Override	Rising edge of PWROK	<p>This signal has a weak internal pull-up.</p> <p>0 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes its fetching the alternate boot block instead of the original boot block. PCH will invert A16 (default) for cycles going to the upper two 64 KB blocks in the NW or the appropriate address lines (A16, A17, A18, A19 or A20) as selected in Top-Swap Block size soft strap (handled through FITC; also see Shark Bay SPI Flash Programming Guide (D10 Book 489495)).</p> <p>1 = Disable "Top Swap" mode.</p> <p>NOTES:</p> <ol style="list-style-type: none">The internal pull-up is disabled after PLTRST# deasserts.Software will not be able to clear the Top Swap mode bit until the system is rebooted.The status of this strap is readable using the Top Swap bit (Chipset Config Registers: RCBA + Offset 3410h:Bit 0).This signal is in the Core well.
DDPS_CTRLDATA	Port B Detected	Rising edge of PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port B is not detected. 1 = Port B is detected.</p> <p>NOTES:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# deasserts.This signal is in the Core well.
DDPC_CTRLDATA	Port C Detected	Rising edge of PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port C is not detected. 1 = Port C is detected.</p> <p>NOTES:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# deasserts.This signal is in the Core well.

Table 2-17. Functional Strap Definitions (Sheet 6 of 6)

Signal	Usage	When Sampled	Comment
DDPD_CTRLDATA	Port D Detected	Rising edge of PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port D is not detected. 1 = Port D is detected.</p> <p>NOTES:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PLTRST# deasserts.This signal is in the Core well.

NOTE: See Section 3.1 for full details on pull-up/pull-down resistors.

<Core Design>

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Title			
PCH (STRAPS)			
Size	Document Number		Rev
Custom	PIM86L-Florence		1
Date:	uesday, February 25, 2011	Sheet	20 of 103

1

A

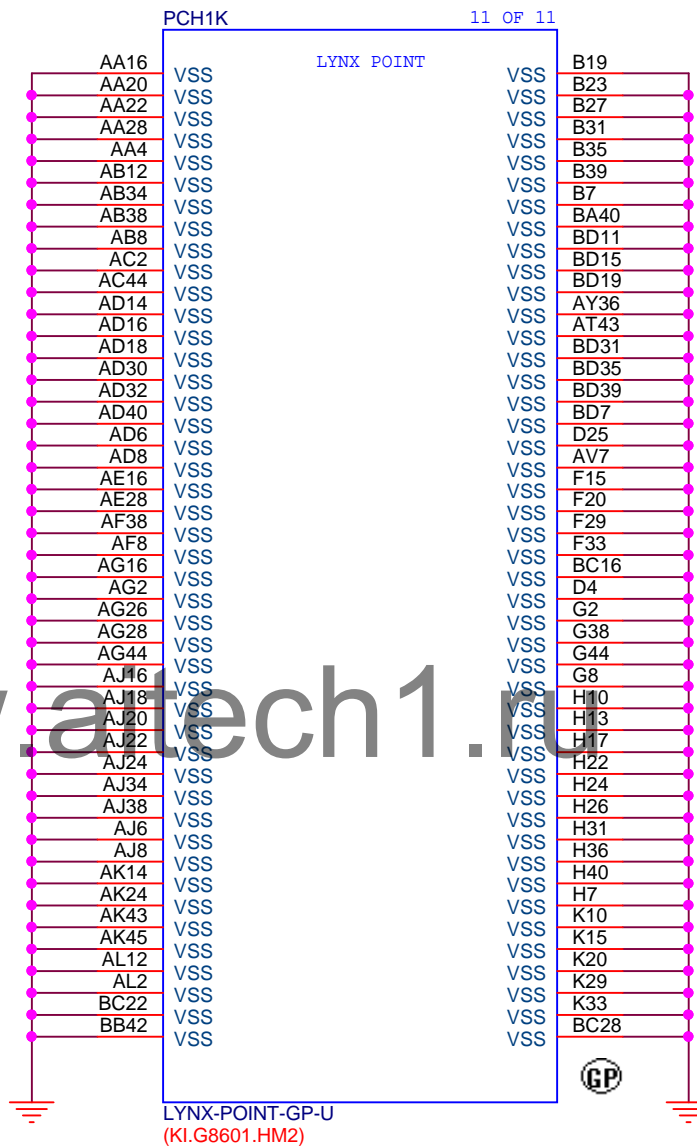
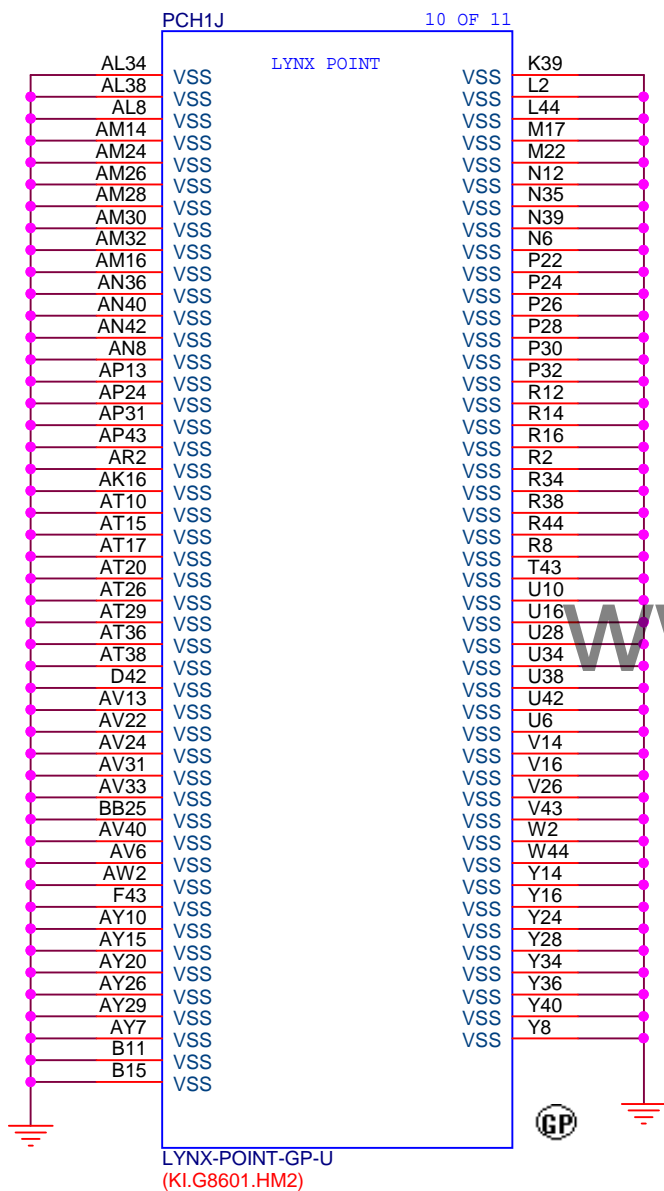
DCPUS1	<p>1.05 V Suspend self power.</p> <p>If INT#PWRN is strapped high then power to this well is supplied internally and this pin should be left as no connect.</p> <p>If INT#PWRN is strapped low then power to this well must be supplied by an external 1.05 V suspend rail.</p> <p>Note: External VR module applies to Mobile Only.</p>
DCPUS5	<p>1.05 V Suspend self power for USB 3.0.</p> <p>If INT#PWRN is strapped high then power to this well is supplied internally and these pins should be left as no connect.</p> <p>If INT#PWRN is strapped low then power to this well must be supplied by an external 1.05 V suspend rail.</p> <p>Note: External VR module applies to Mobile Only.</p>



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SSID = PCH



<Core Design>

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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Kinetics	45	3	123-135
2. Kinetic Analysis of the Decomposition of Hydrogen Peroxide	Jane Smith	2019	International Journal of Chemical Kinetics	52	1	45-58
3. The Influence of Catalyst Concentration on Reaction Rate	Michael Chen	2020	Journal of Physical Chemistry	124	2	789-801
4. Kinetic Modeling of the Reaction Between Nitrogen Dioxide and Carbon Monoxide	Sarah Johnson	2021	Environmental Science and Technology	55	4	2345-2358
5. The Role of Solvent Polarity in the Rate of Nucleophilic Substitution	David Lee	2022	Journal of Organic Chemistry	87	5	1567-1580

PCH (VSS)

Size
A

Document Number

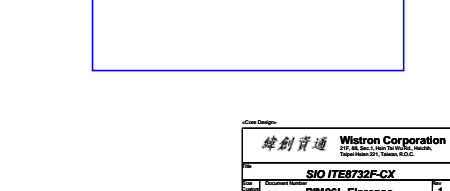
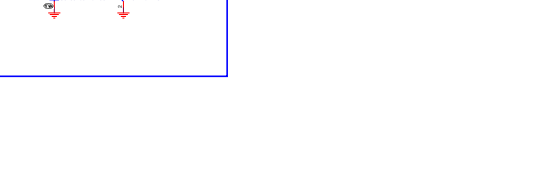
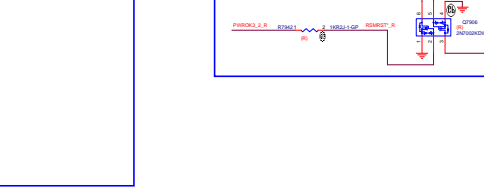
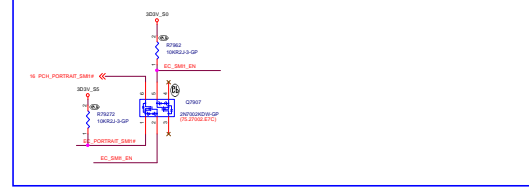
Rev

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1

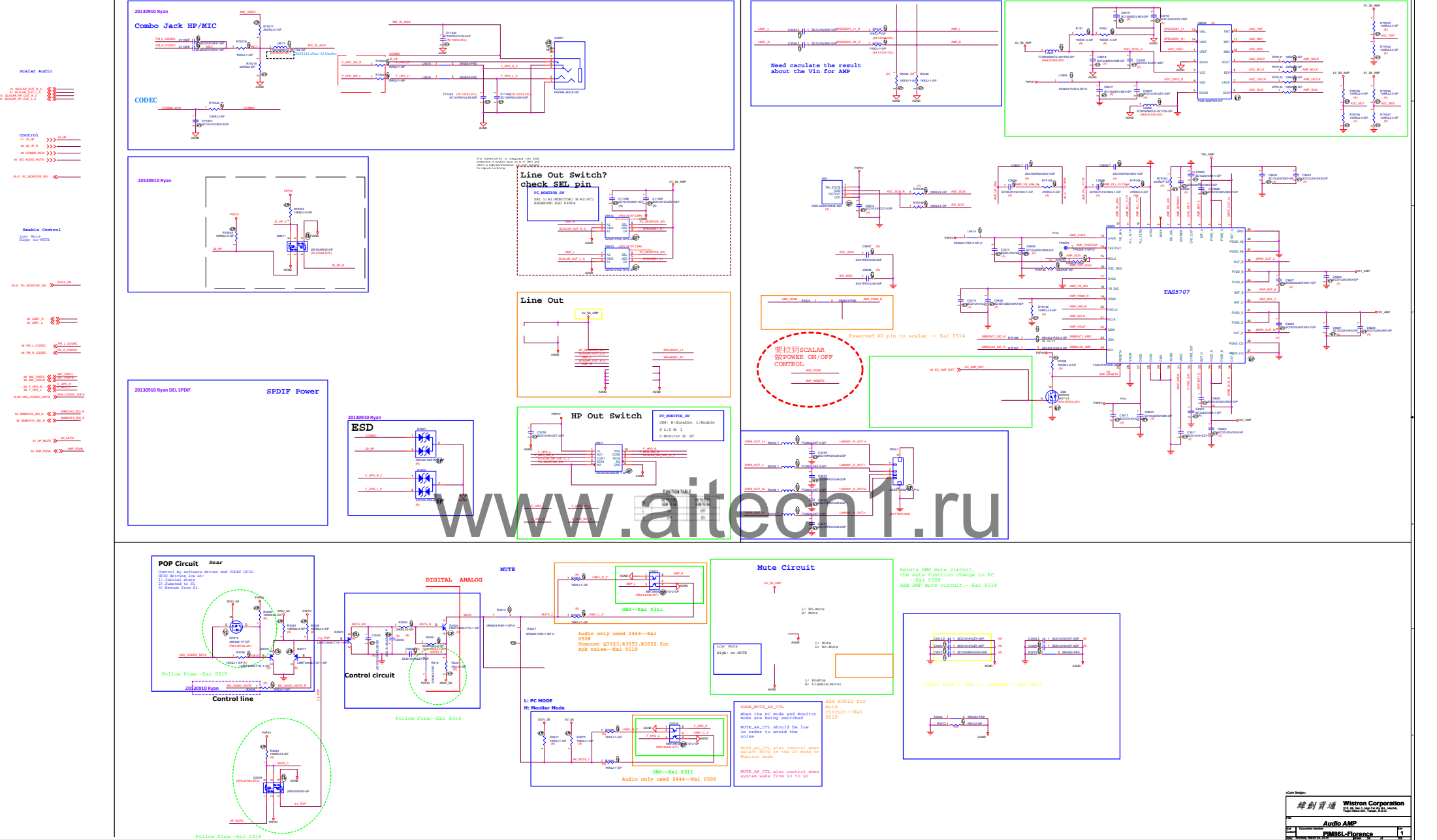
Date: Tuesday, February 25, 2014

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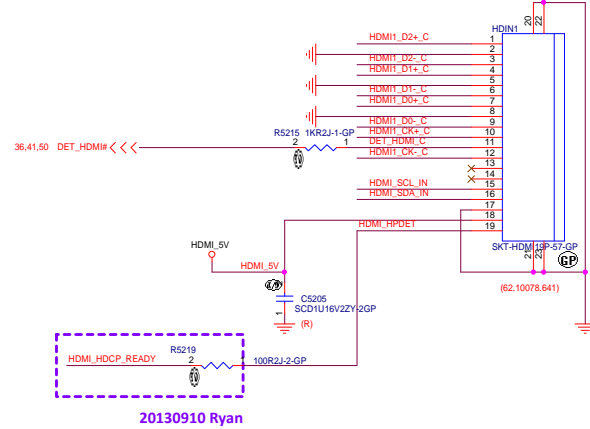
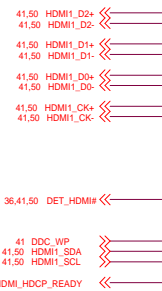


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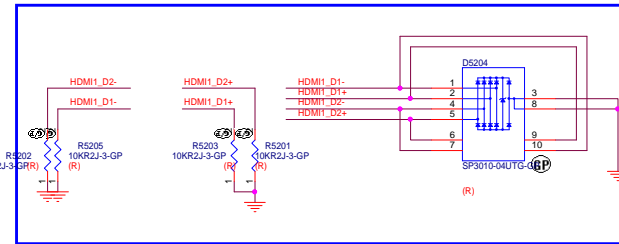
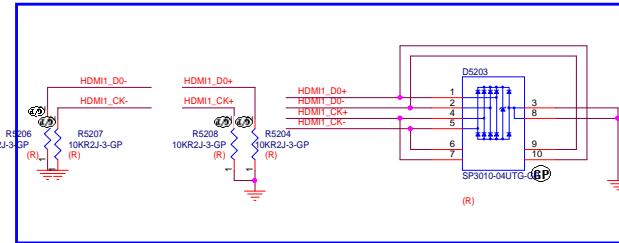
HDMI-IN

Connector

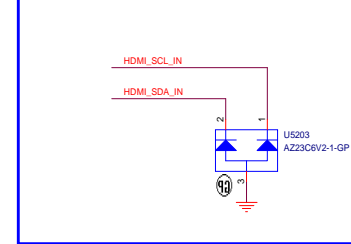
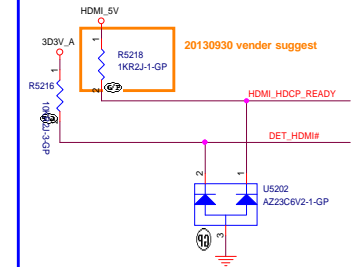
HDMI



EMI/ESD near Connector

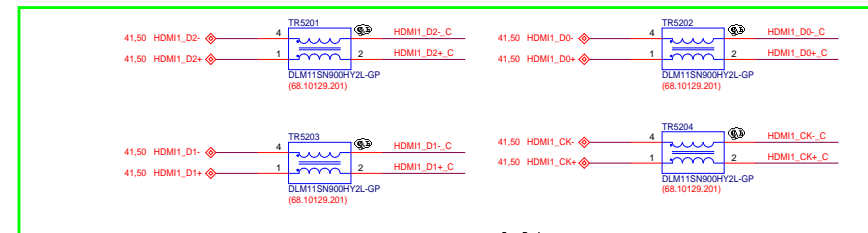
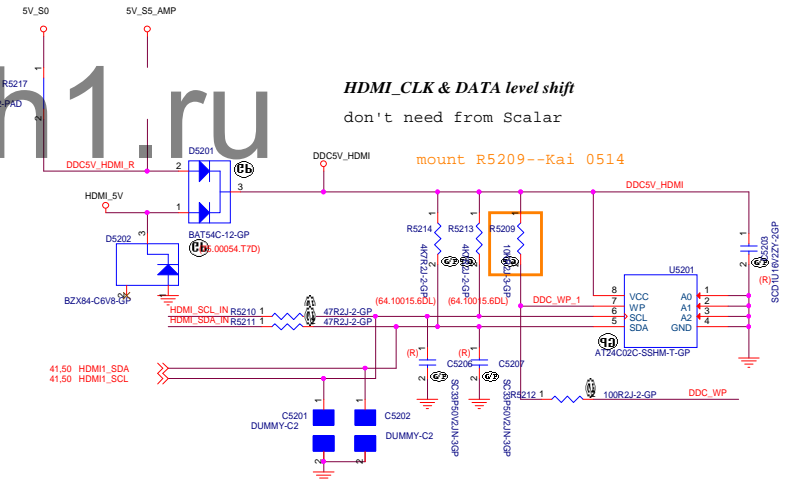


EMI/ESD near Connector



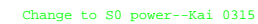
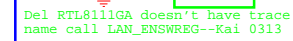
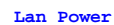
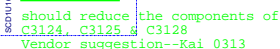
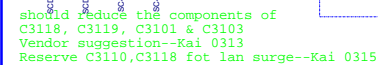
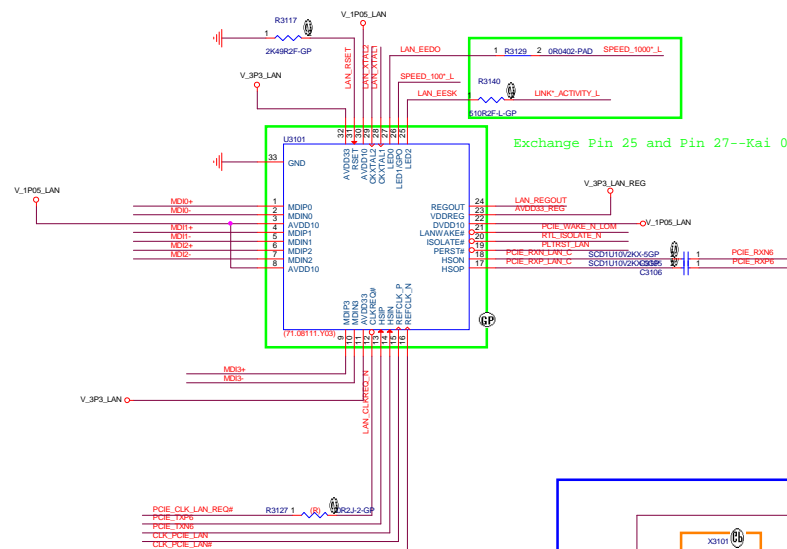
HDMI_MHL switch circuit

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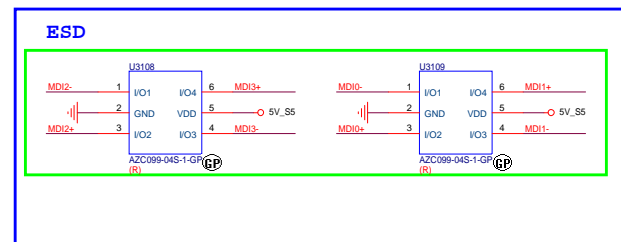
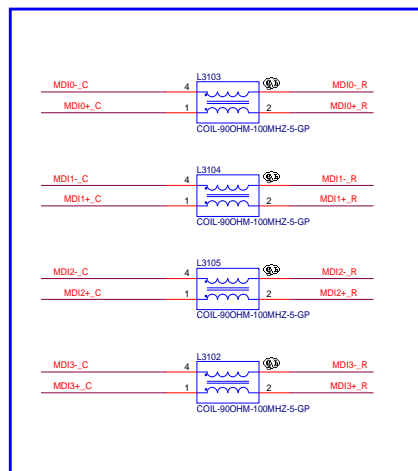
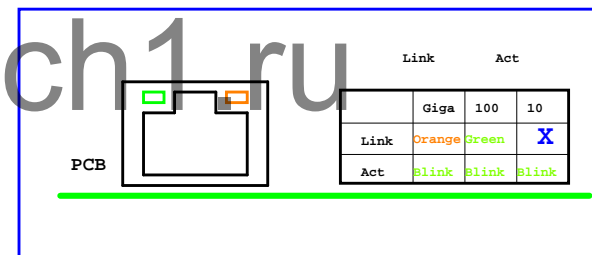
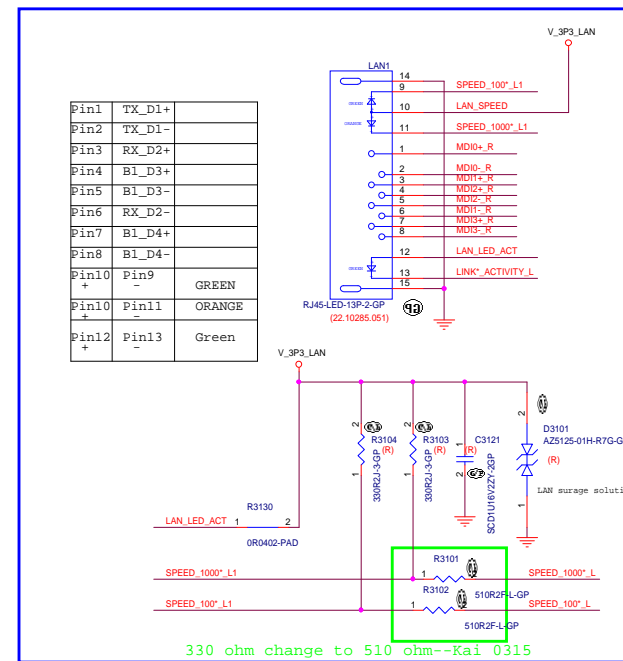
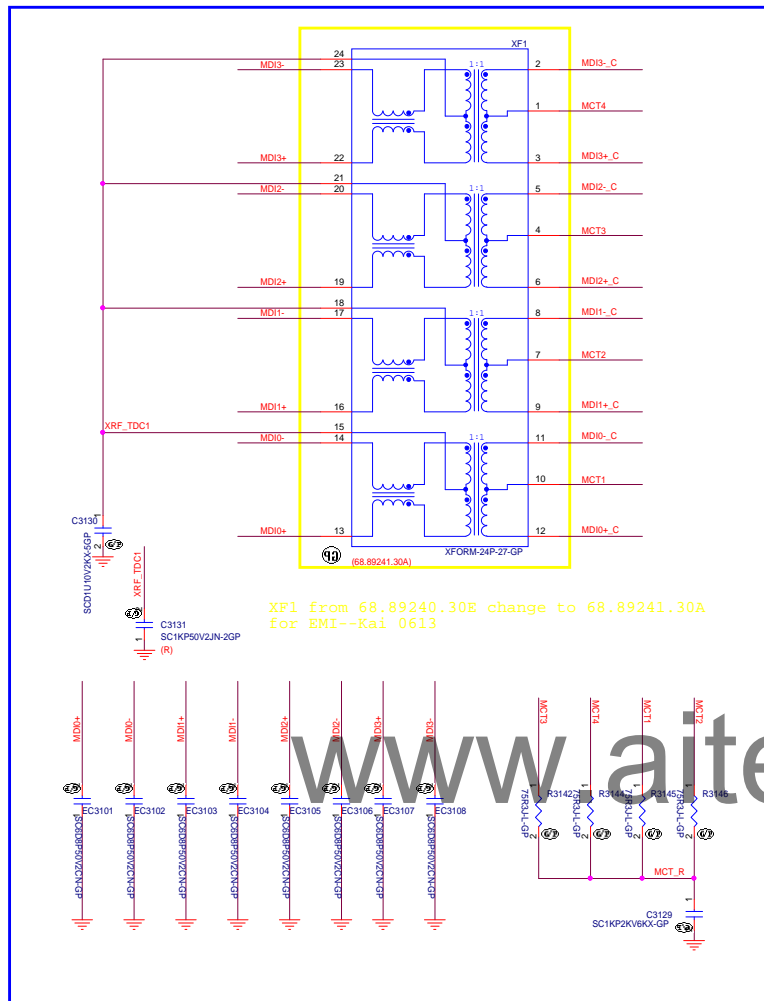


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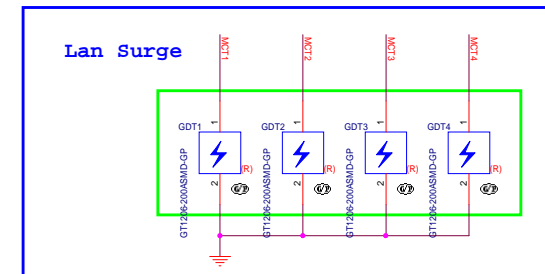
HDMI IN		
Size C	Document Number	Rev 1
PIM86L-Florence		
Date: Tuesday, February 25, 2014	Sheet 29	of 103



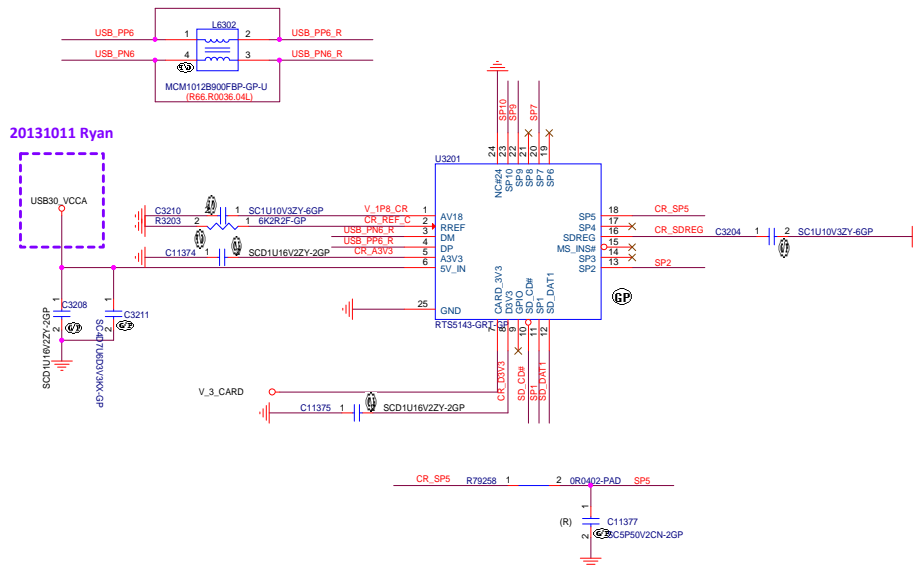
30 MDIO+
30 MDIO-
30 MDI1+
30 MDI1-
30 MDI2+
30 MDI2-
30 MDI3+
30 MDI3-
30 SPEED_1000*_L
30 SPEED_100*_L
30 LINK*_ACTIVITY_L



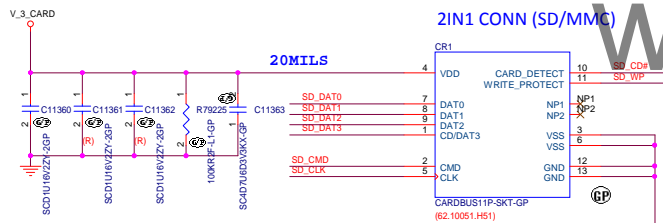
Unmount U3108 and U3109--Kai 0308
OBS--Kai 0311



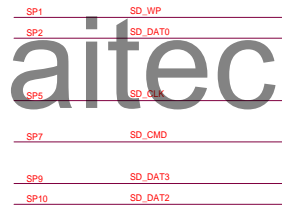
(MS / SD / MMC)



20130910 Ryan



2IN1 (SD/MMC) Combo Net



<Variant Name>

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File

RTS5143 (CARD READER)

Size

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Rev

1

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<Variant Name>

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

CARD Reader CONN

Size
B

Document Number
PIM86L-Florence

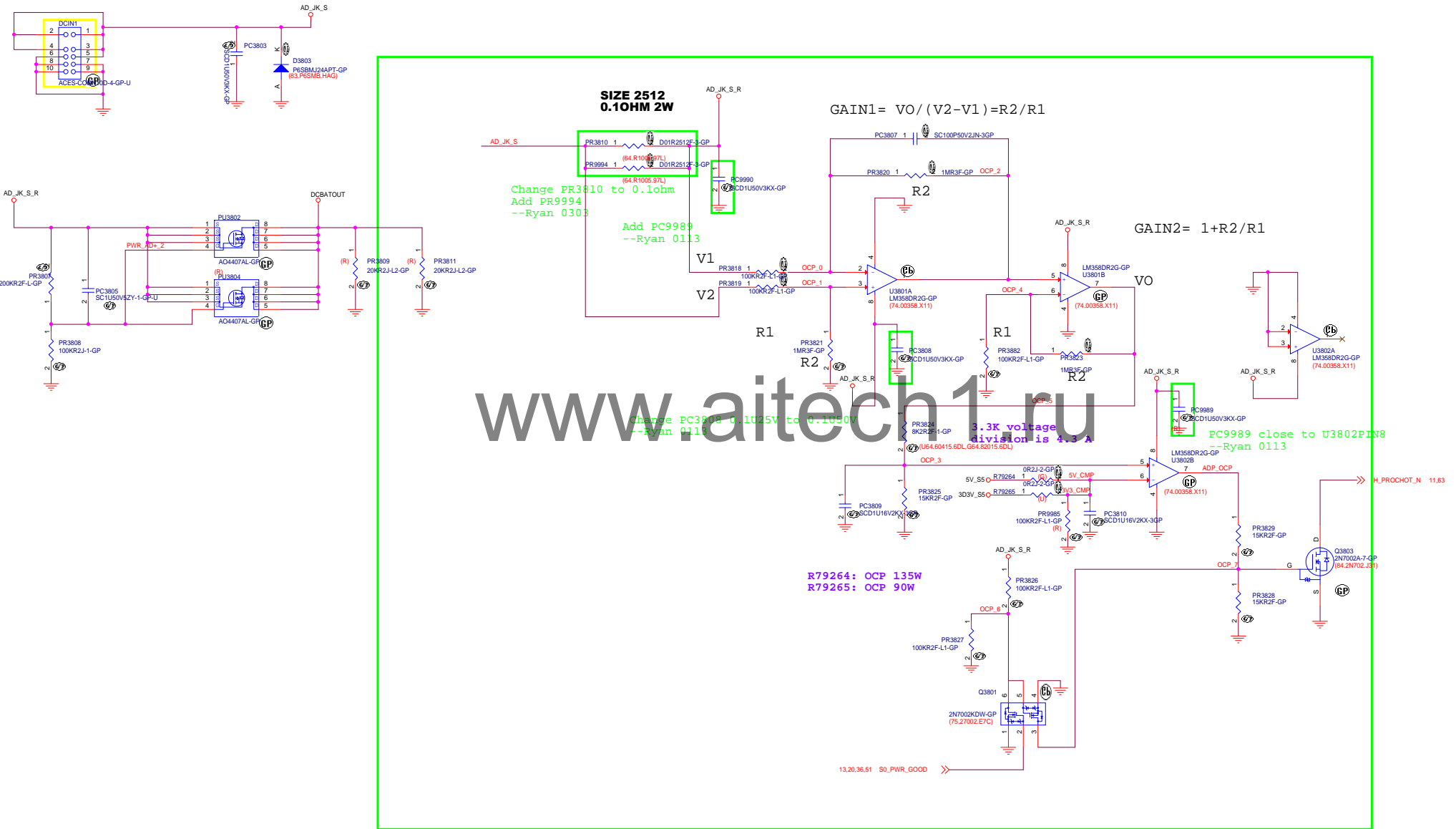
Rev
1

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ANNIE solution

DCIN1 from 20.81884.010 change to 20.81633.010-- Kai 0610



HR PX

緯創資通 Wistron Corporation
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DCIN JACK			
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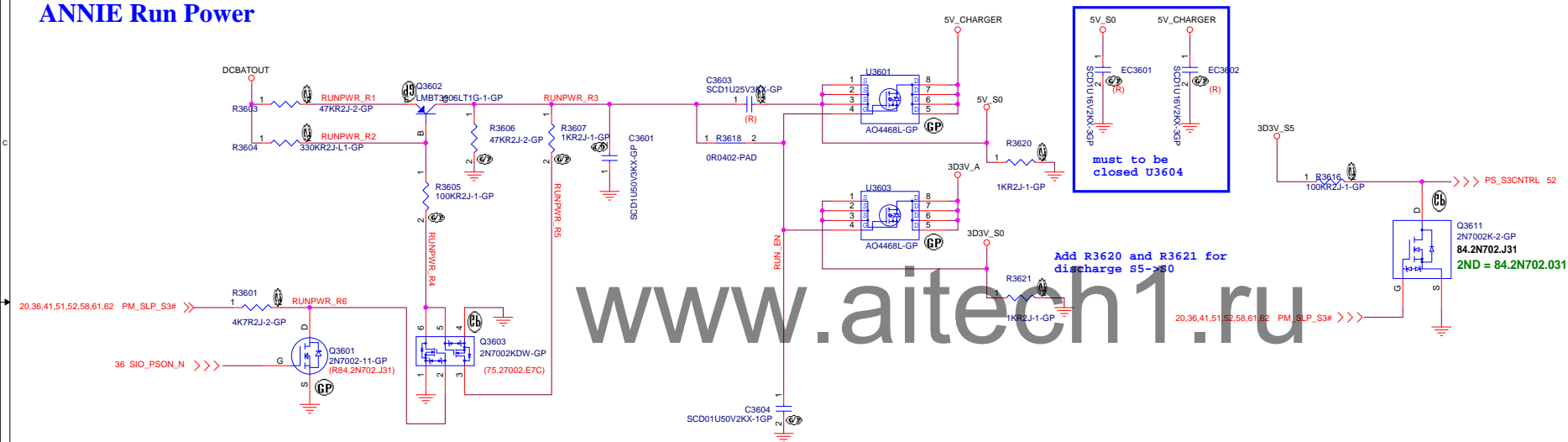
Power Sequence

From short pad to 0 ohm,Reserved for sequence --Kai 0723

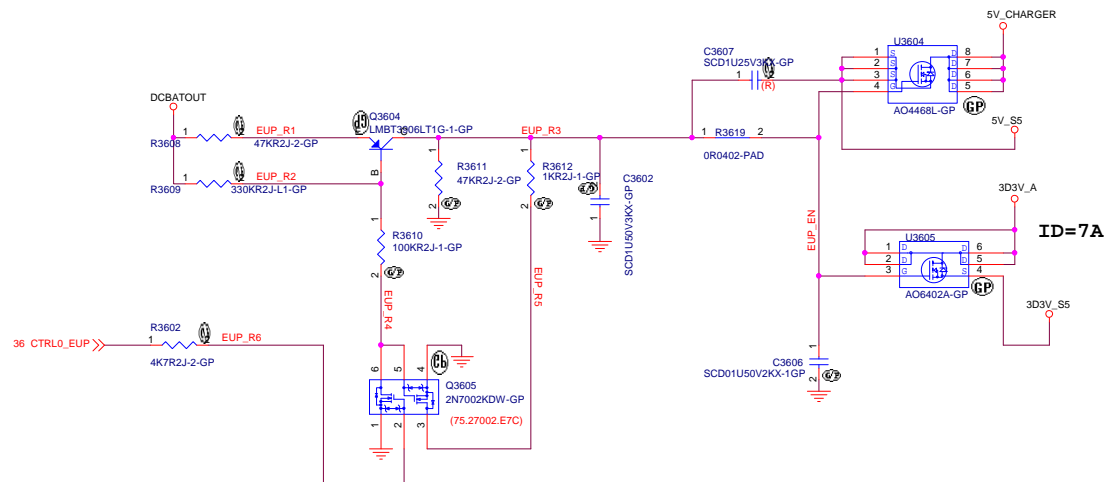


*Reserve for
system power
ok*

ANNIE Run Power



EUP Power



ID=7A

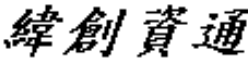
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Run Power & Sequence			
Size	Document Number	Rev	
Custom	PIM86L-Florence	1	
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<Core Design>

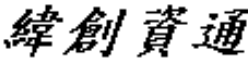
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Title			
1D05 M			
Size	Document Number		Rev
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AO3418 NMOS 3.1A, 60mohm,Vgs=10V
NMOS H: Enable L:Disable
3.1A 60 mohm(10V)
(Vds 30V,Vgs 12V)



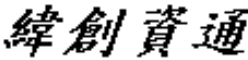
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Title			
Connected Standby			
Size A	Document Number PIM86L-Florence		Rev 1
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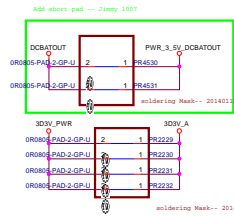
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Title			
DCIN JACK			
Size A	Document Number		Rev
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BATT CONN			
Size A	Document Number		Rev
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3D3V_PWR / 5V_PWR



PWR_3_5V_DCBATOUT VIN RIPLE CURRENT Imax=2.84A

84.08884.037 FDS8884
Vgs @ 4.5V,
Id = 8.5A,
Rds(on) = 23.0~30.0mohm,
Qg = 5~7nC

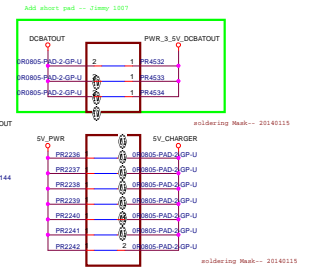
84.06690.G37 FDS6690AS
Vgs @ 4.5V,
Id = 10A,
Rds(on) = 12~15mohm,
Qg = 9~13nC

084.00472.0037 SIR472DP
Vgs @ 4.5V,
Id = 18A,
Rds(on) = 9-11.5mohm,

84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4-6.0mohm,

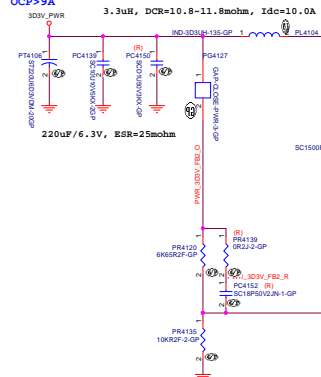
84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4-6.0mohm,

VIN RIPPLE CURRENT $I_{max}=4.85A$



I_{omax}=7.5A
OCP>9A

3.3uH, DCR=10.8~11.8mohm, Idc=10.0A

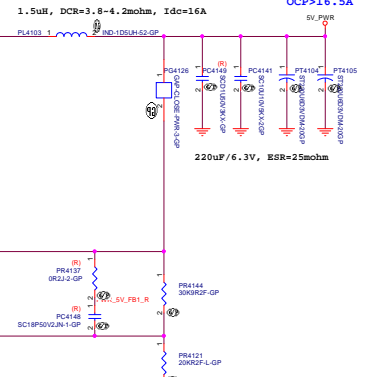

$$\Delta I = \frac{(V_{in} - V_{out}) \cdot V_{out}}{(V_{in} \cdot L \cdot F_{sw})}$$

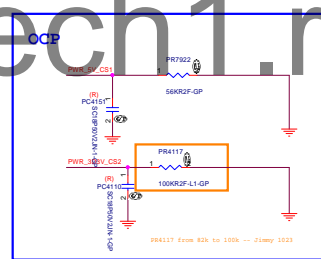
$$\Delta I = \frac{(19 - 3) \cdot 3}{(19 \cdot 3\mu \cdot 350K)} = 2.36A$$

Frequency	300k/CH1 350k/CH2
-----------	----------------------

1.5uH, DCR=3.8-4.2mohm, Idc=16A

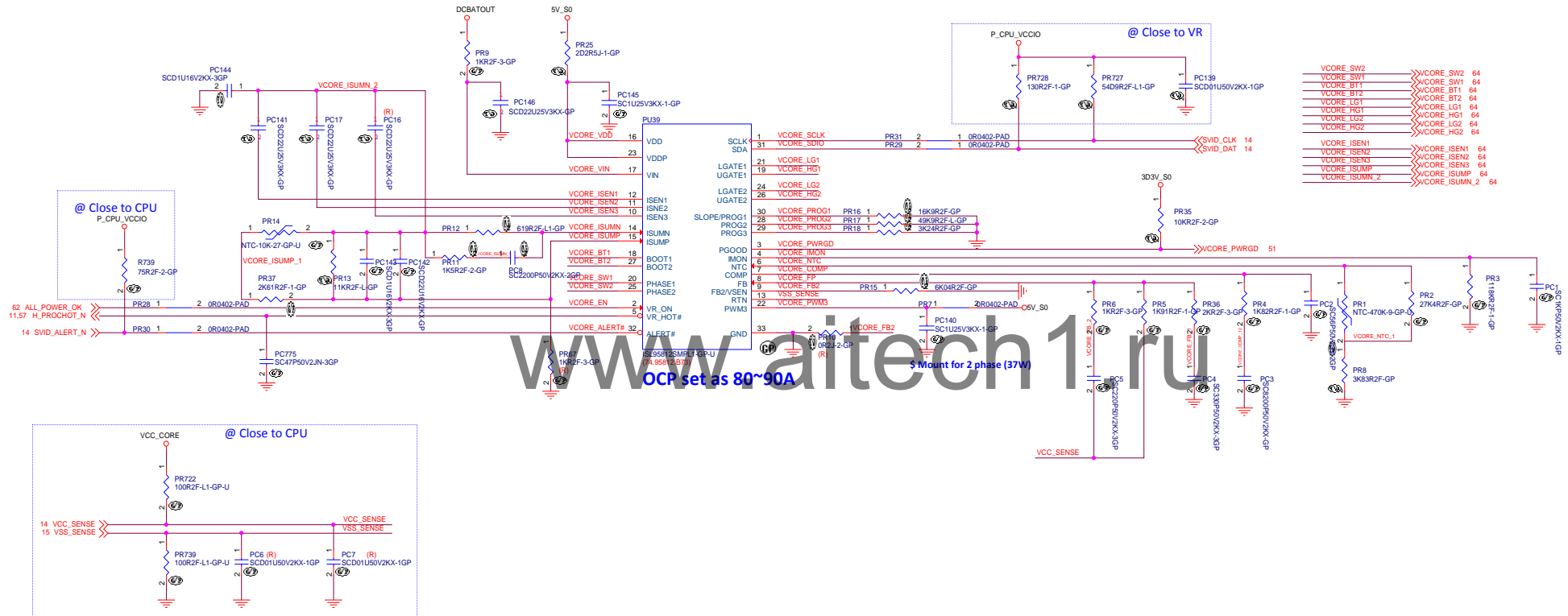
Iomax=11A
OCP>16.5A


$$\Delta I = \frac{(V_{in} - V_{out}) * V_{out}}{(V_{in} * L * F_{sw})}$$

$$\Delta I = \frac{(19 - 5) * 5}{(19 * 1.5u * 300K)} = 8.2A$$


TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only



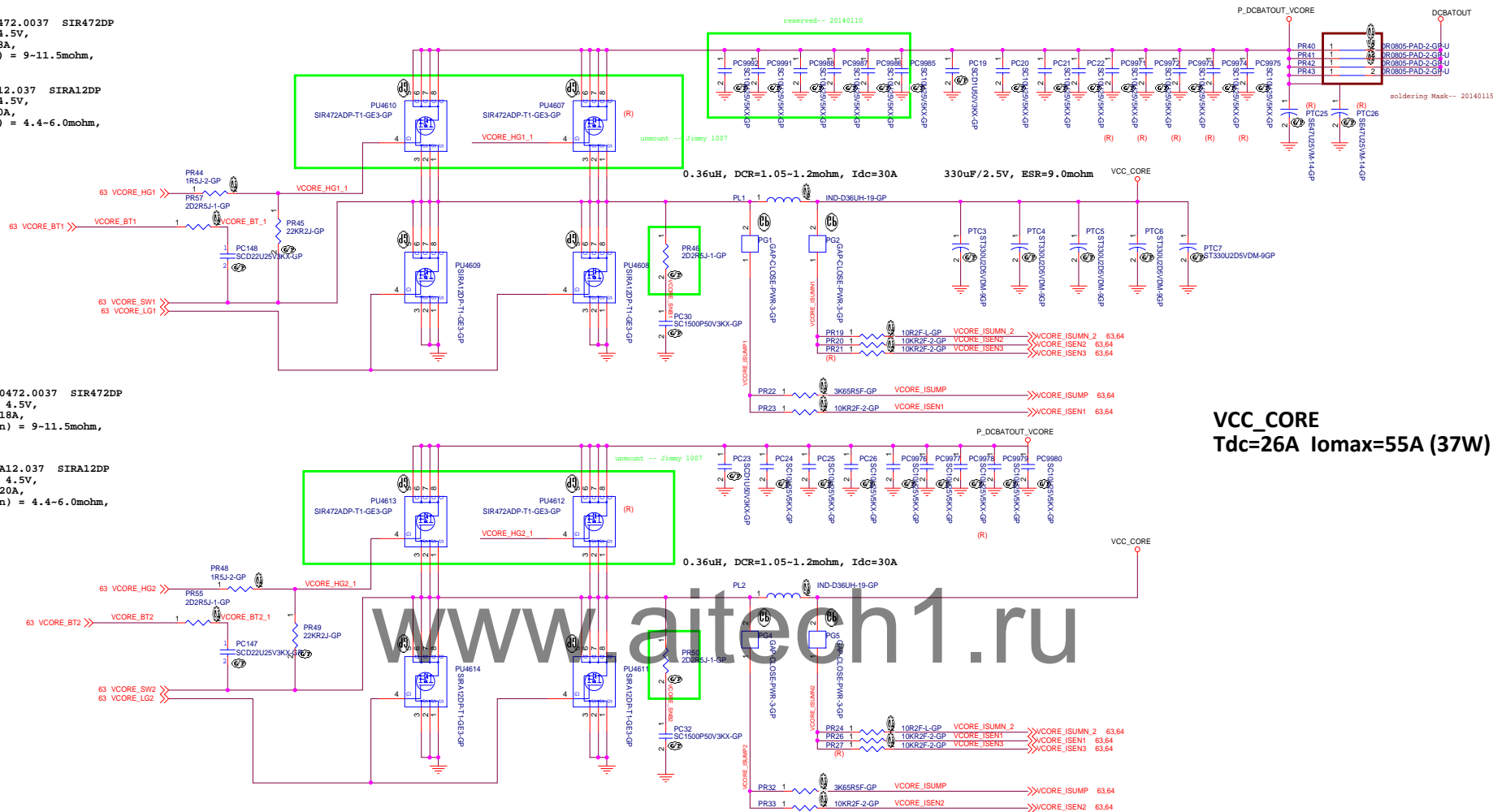
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- VCORE_SW1 >>> VCORE_SW1 64
- VCORE_BT1 >>> VCORE_BT1 64
- VCORE_BT2 >>> VCORE_BT2 64
- VCORE_LG1 >>> VCORE_LG1 64
- VCORE_HG1 >>> VCORE_HG1 64
- VCORE_LG2 >>> VCORE_LG2 64
- VCORE_HG2 >>> VCORE_HG2 64
- VCORE_ISEN1 >>> VCORE_ISEN1 64
- VCORE_ISEN2 >>> VCORE_ISEN2 64
- VCORE_ISEN3 >>> VCORE_ISEN3 64
- VCORE_ISUMP >>> VCORE_ISUMP 64
- VCORE_ISUMN_2 >>> VCORE_ISUMN_2 64

084.00472.0037 SIR472DP
Vgs @ 4.5V,
Id = 18A,
Rds(on) = 9~11.5mohm,

84.SRA12.037 SIRAI2DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4~6.0mohm,

084.00472.0037 SIR472DP
Vgs @ 4.5V,
Id = 18A,
Rds(on) = 9~11.5mohm,

84.SRA12.037 SIRAI2DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4~6.0mohm,



VCC_CORE
Tdc=26A Iomax=55A (37W)

DISABLE PWM3

<Variant Name>

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084.00472.0037 SIR472DP
 Vgs @ 4.5V,
 Id = 18A,
 Rds(on) = 9~11.5mohm,

VIN RIPLE CURRENT I_{max}=2.52A

I_{omax}=11A
 OCP>16.5A

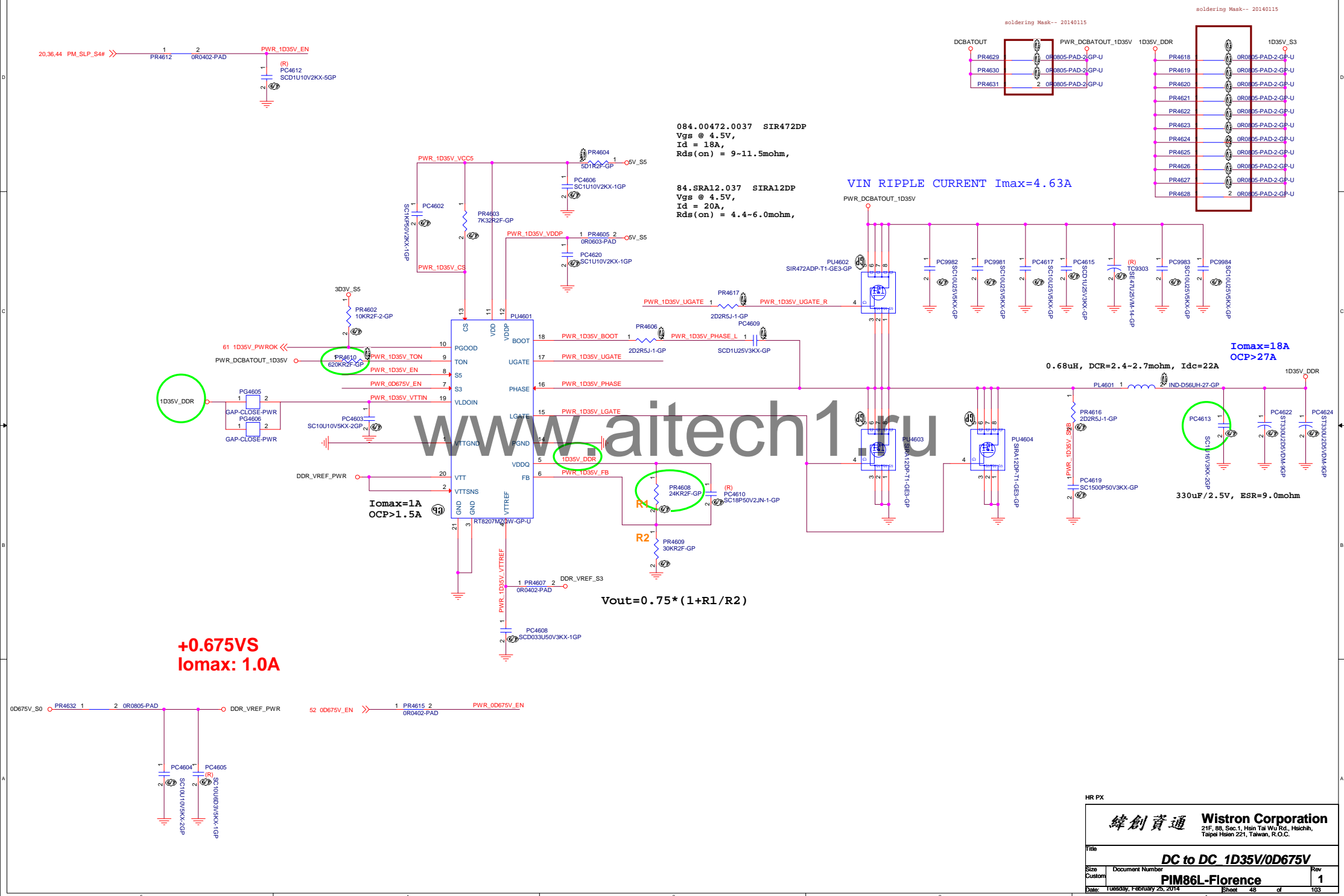
$$V_{OUT} = ((R1+R2)/R2) * 0.7$$

HR PX

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SSID = PWR.Plane.Regulator_1p5v0p75v



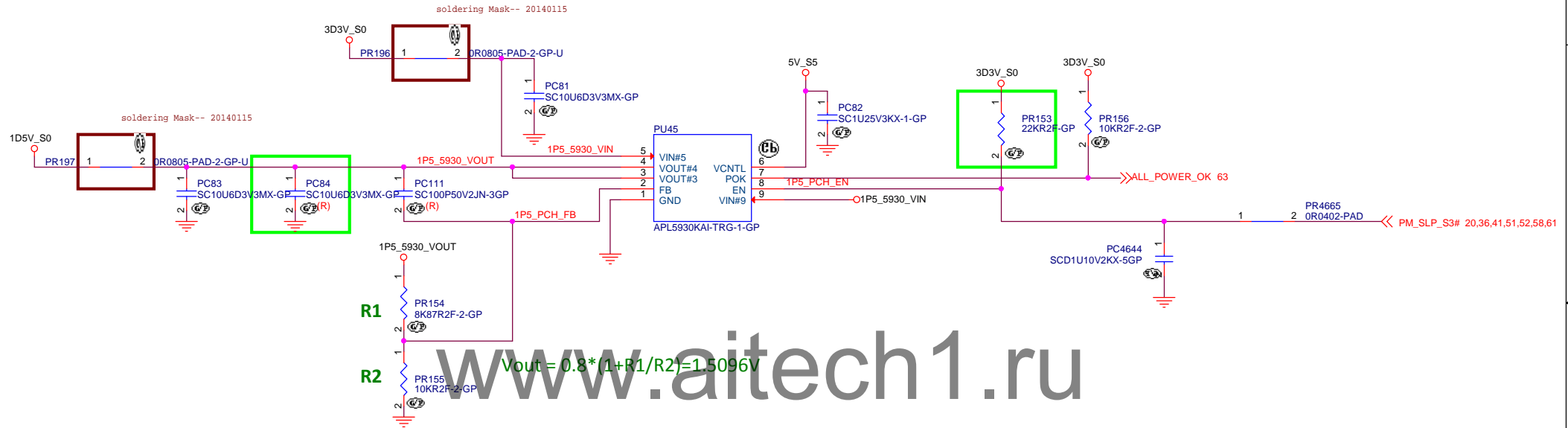
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title DC to DC_1D8V			
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1D5V_S0
MAX=1A

Delete 1D5V_S0_VGA--Kai 0321



<Variant Name>

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Title

DC to DC 1D5V(APL5930)

Size

Document Number

B

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1

Date:

Tuesday, February 25, 2014

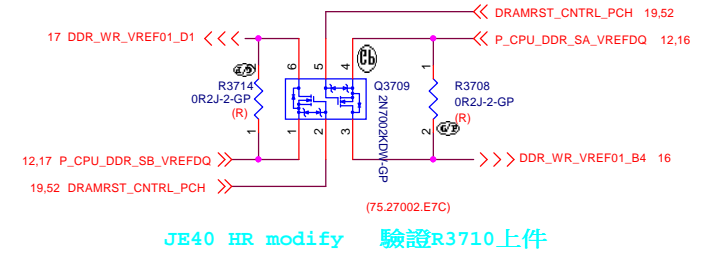
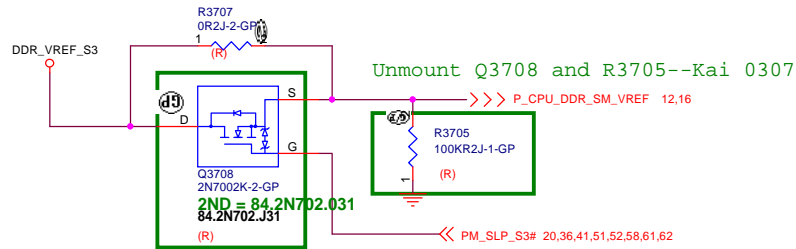
Sheet

50

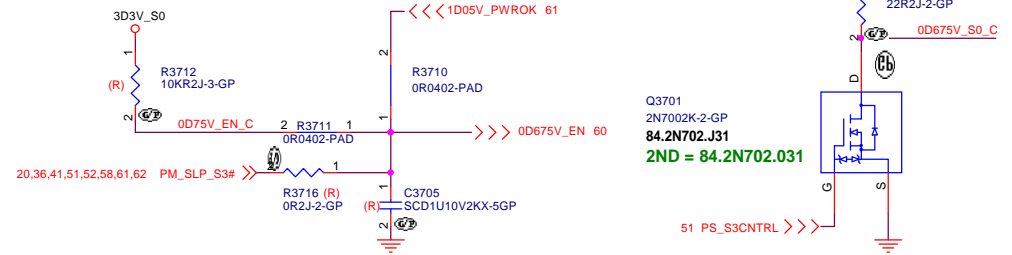
of

103

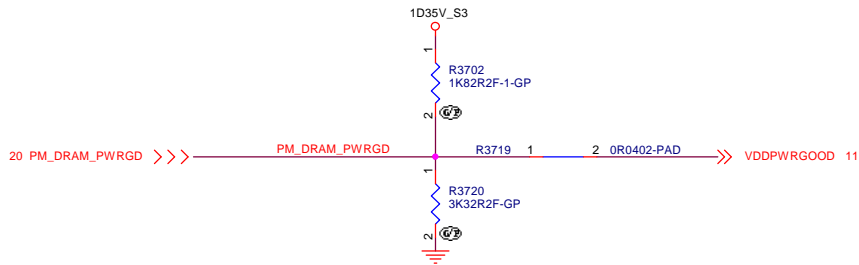
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



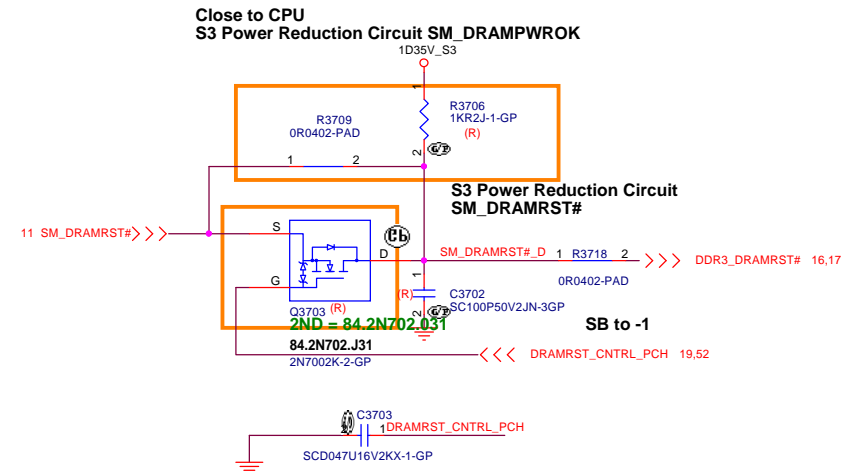
5 S3 Power Reduction X01 20091111

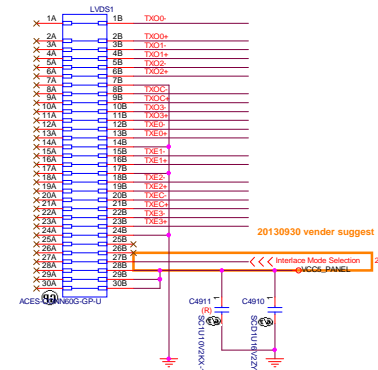
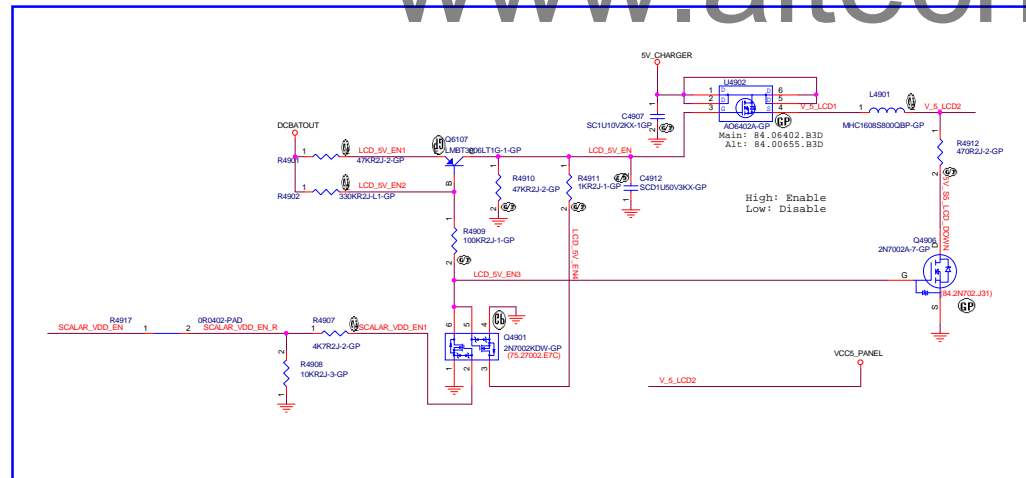
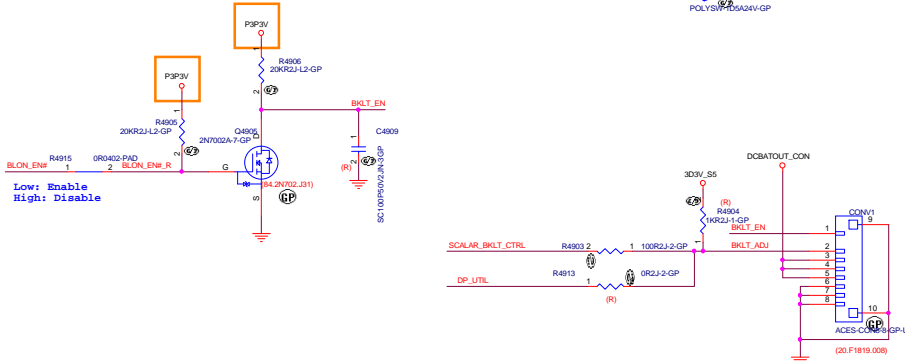
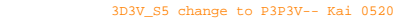


SM_DRAMPWROK Topology for platforms not supporting Deep S3



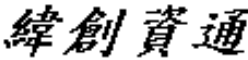
Unmount Q3703 and R3706, mount R3709--Kai 0524





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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CRT Board Connector			
Size A	Document Number		Rev
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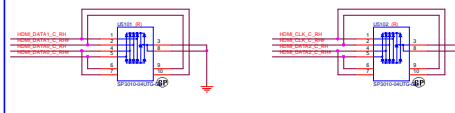
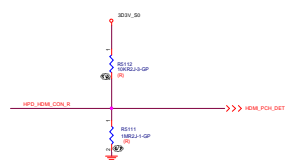
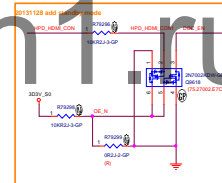
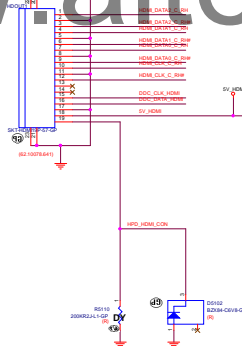
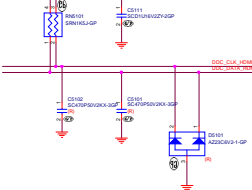
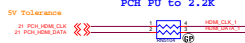
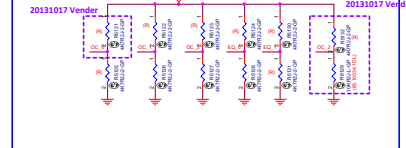
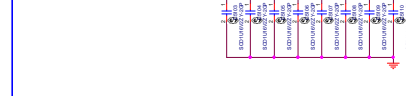
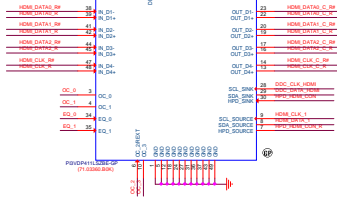
SSID = VIDEO

UMA_Muxless : default setting used PS8101.
please change C5103-C5110 to 0 ohm resistor



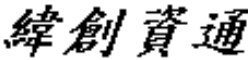
71.03411.D03	Low	Low	NC	NC	NC	NC
NXP	Bq	NC	NC	NC	NC	NC

Eg : Check SW



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HR PX

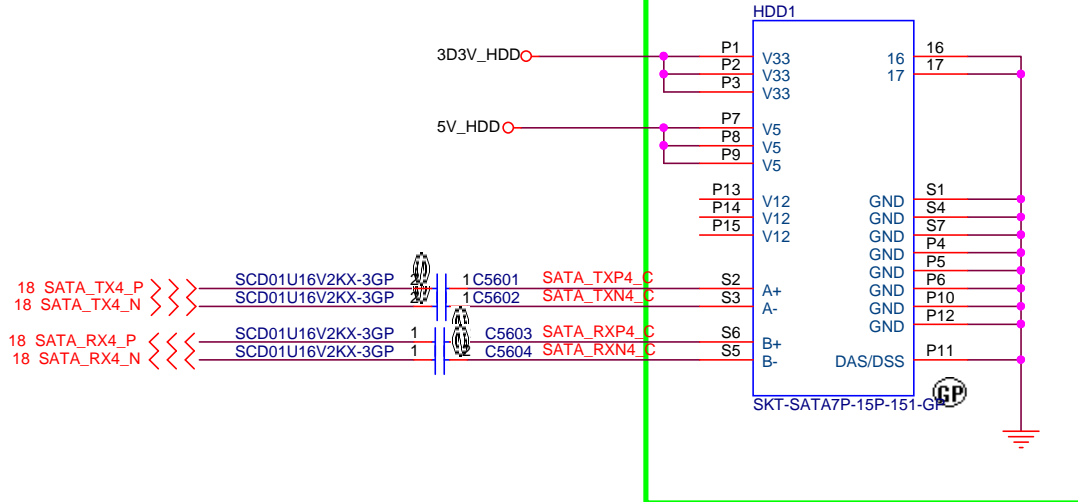
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Display Port			
Size A	Document Number		Rev
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SSID = SATA

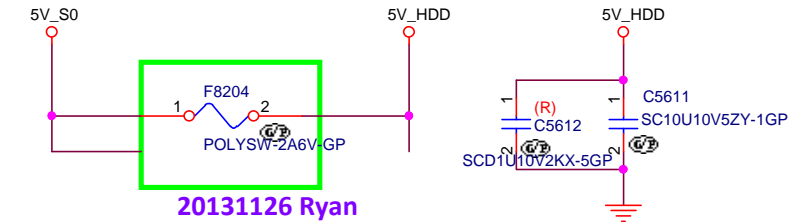
SATA HDD Connector

20130926 Ryan

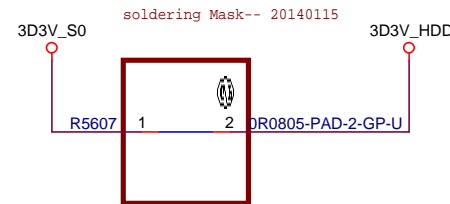
20131015 Ryan



Layout: Put them together

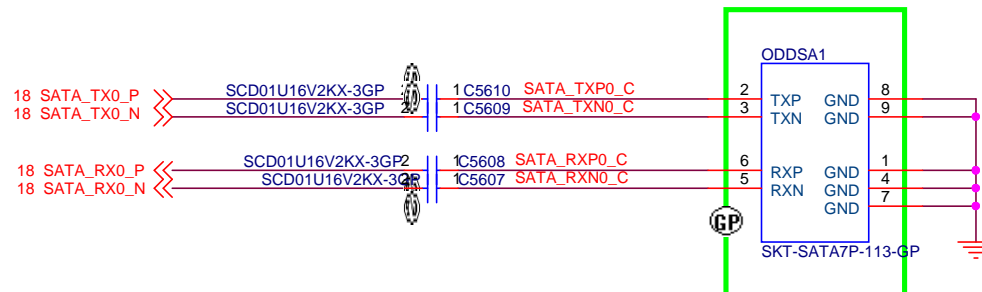


20131126 Ryan

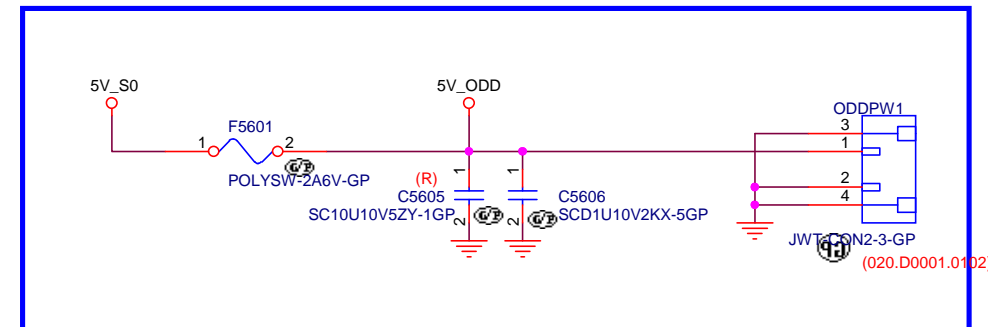


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ODD Connector



20131126 Ryan

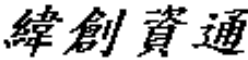


<Core Design>

<p>緯創資通 Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title</p> <p>HDD/ODD</p>	
<p>Size</p> <p>Custom</p>	<p>Document Number</p> <p>PIM86L-Florence</p>
<p>Date:</p> <p>Tuesday, February 25, 2014</p>	<p>Rev</p> <p>1</p>
<p>Sheet 56 of 103</p>	

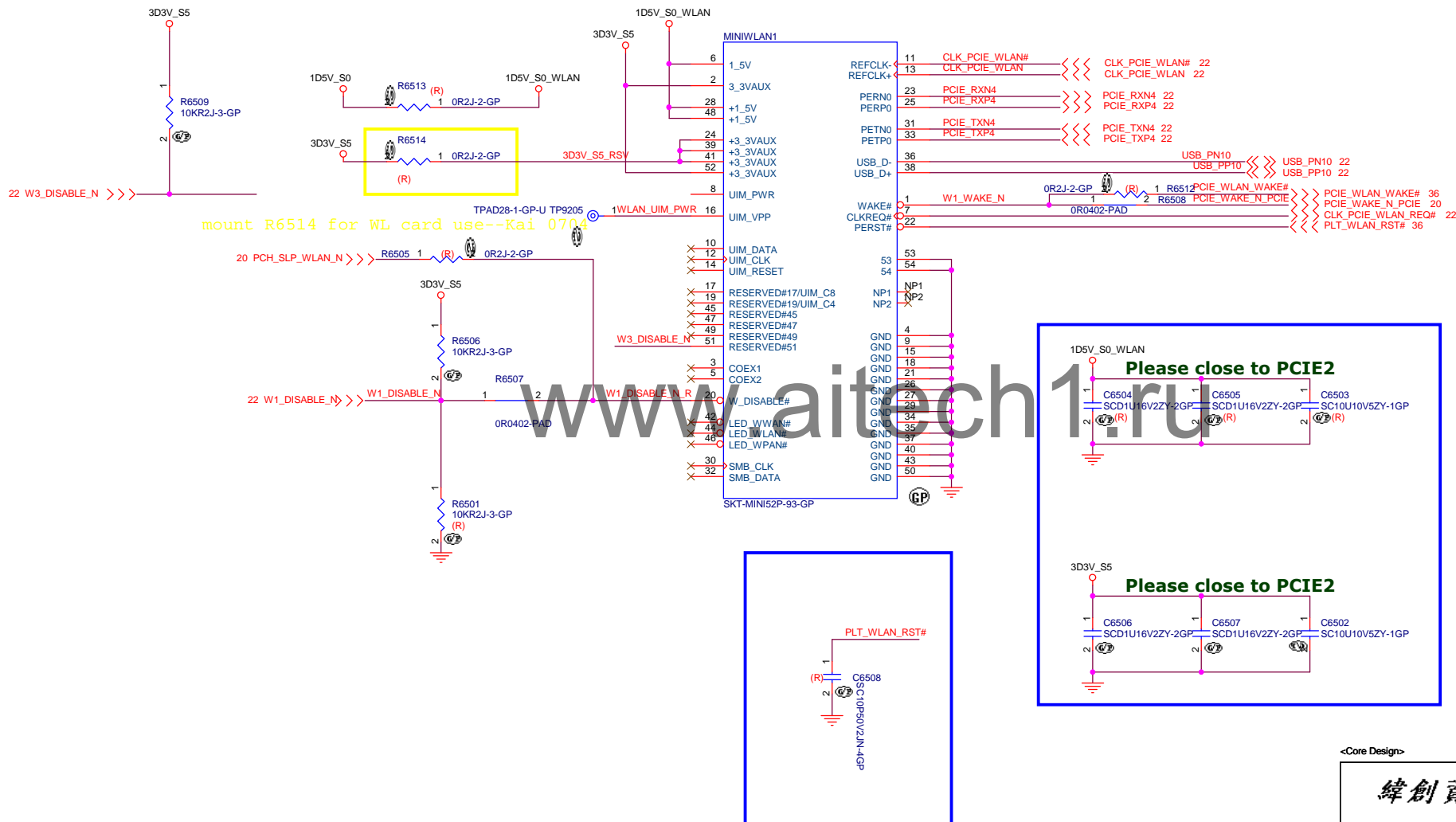
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title E-SATA			
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SSID = Wireless and Bluetooth

Mini Card Connector(Wireless LAN+BT)



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Mini PCIE Card WLAN and BT

Size
Custom

Document Number

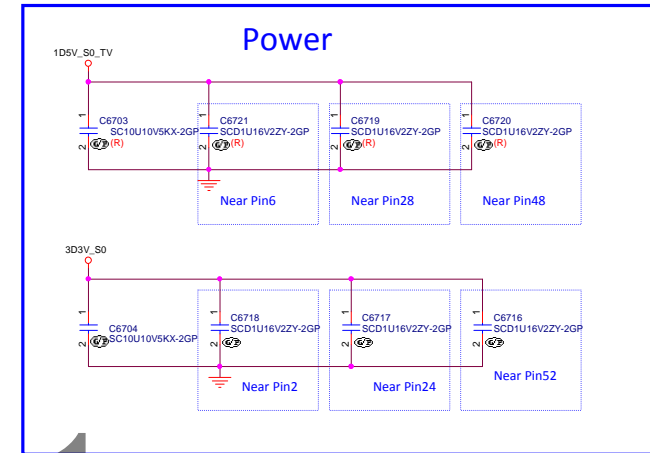
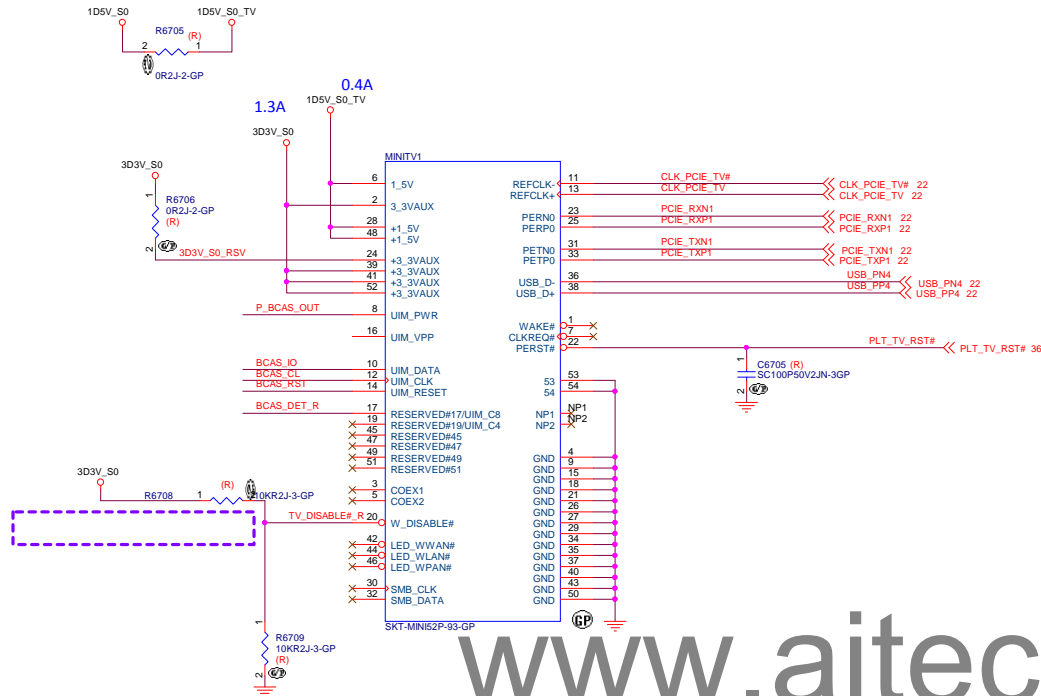
PIM86L-Florence

Rev
1

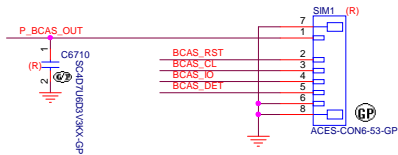
Date: Tuesday, February 25, 2014

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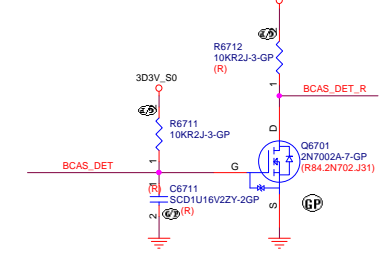
Mini Card Connector (TV Tuner)



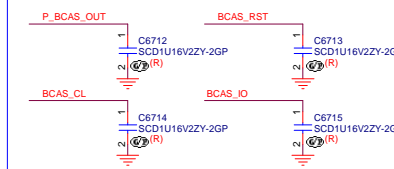
B-CAS Connector SIM1



B-CAS Card Detect



SIM EMI



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

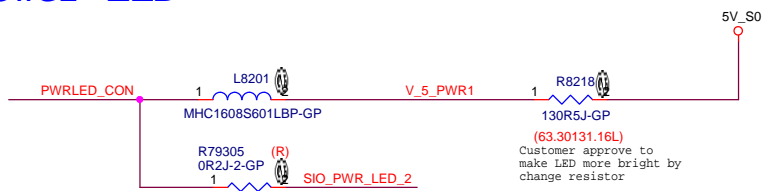
Title			
Mini PCIE Card (TV & SIM)			
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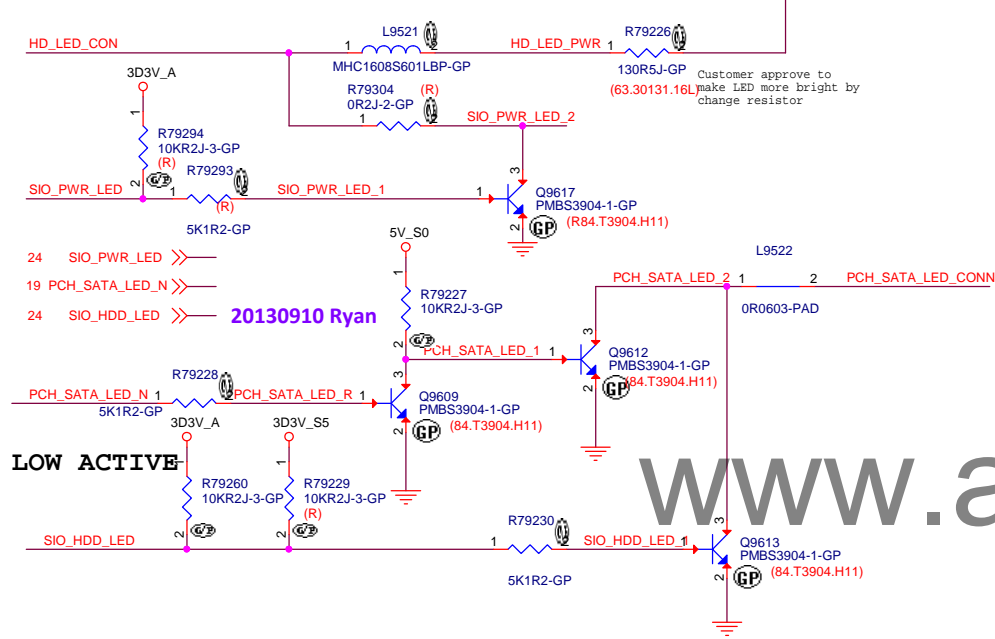
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Mini PCIE Card mSATA			
Size	Document Number		Rev
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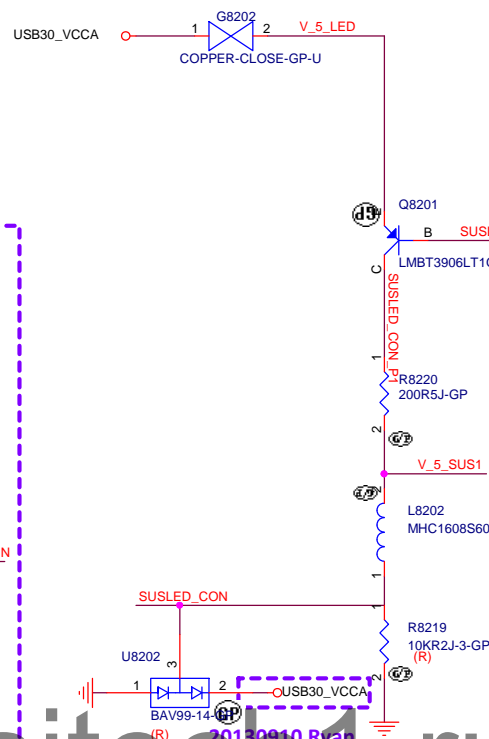
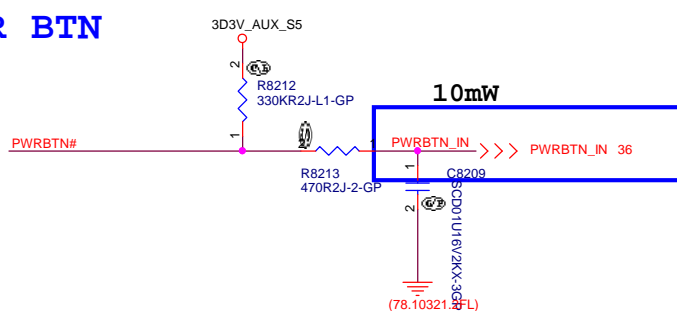
Power LED



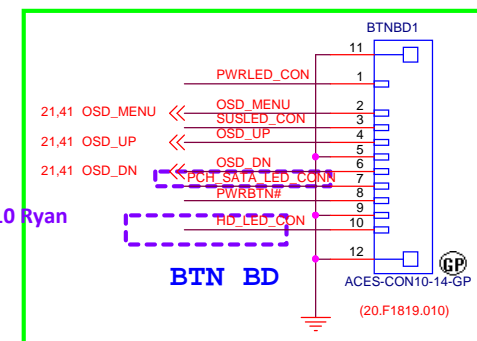
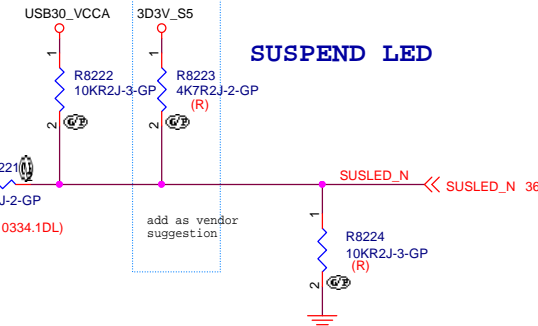
HDD LED



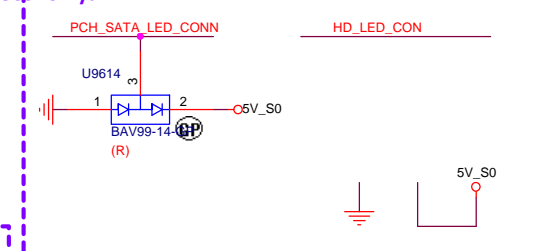
PWR BTN



SUSPEND LED



20130910 Ryan



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緯創資通 Wistron Corporation
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Title		
PWR BT/Side Key/LED		
Size	Document Number	Rev
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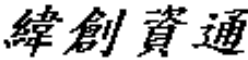
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<Core Design>

<div>緯創資通</div>		<div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title			
<div>Key Board/Touch Pad</div>			
Size A	Document Number		Rev
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Date:	Tuesday, February 25, 2014	Sheet 62 of	103

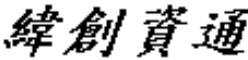
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title IO Board Connector			
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Hall Sensor			
Size A	Document Number		Rev
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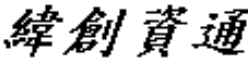
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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>PWR BT/Side Key/LED</i>			
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>PWR BT/Side Key/LED</i>			
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Q2001 Q2002 Q2201 Q3009 Q3012 Q3603 Q3605 Q3608 Q3709 Q3801
Q4901 Q6101 Q7905 Q9301 Q9501 Q9502 Q9503 Q9504 Q9603 84 change
to 75--Kai 0513

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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Bug/BOM issue

Size

A

Document Number

PIM86L-Florence

Rev

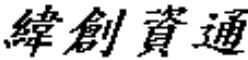
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Date: Tuesday, February 25, 2014

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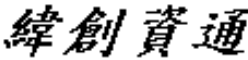
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Title			
<i>PWR BT/Side Key/LED</i>			
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A	PIM86L-Florence		1
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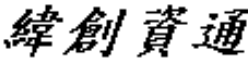
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>PWR BT/Side Key/LED</i>			
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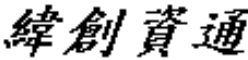
www.aitech1.ru

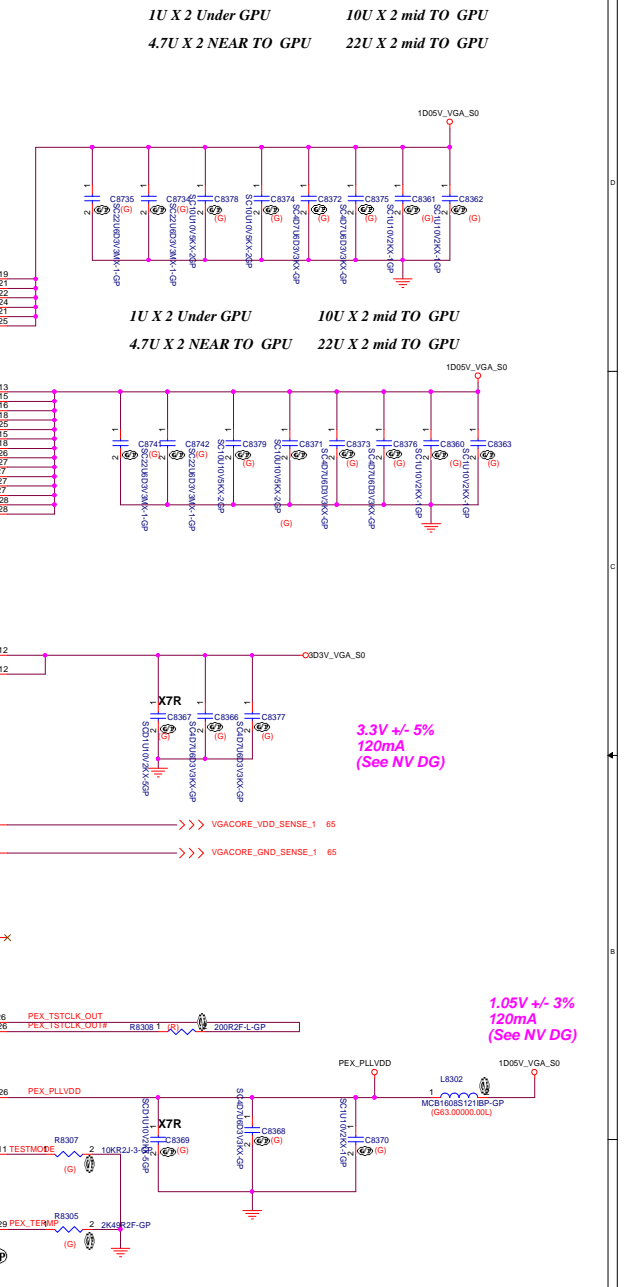
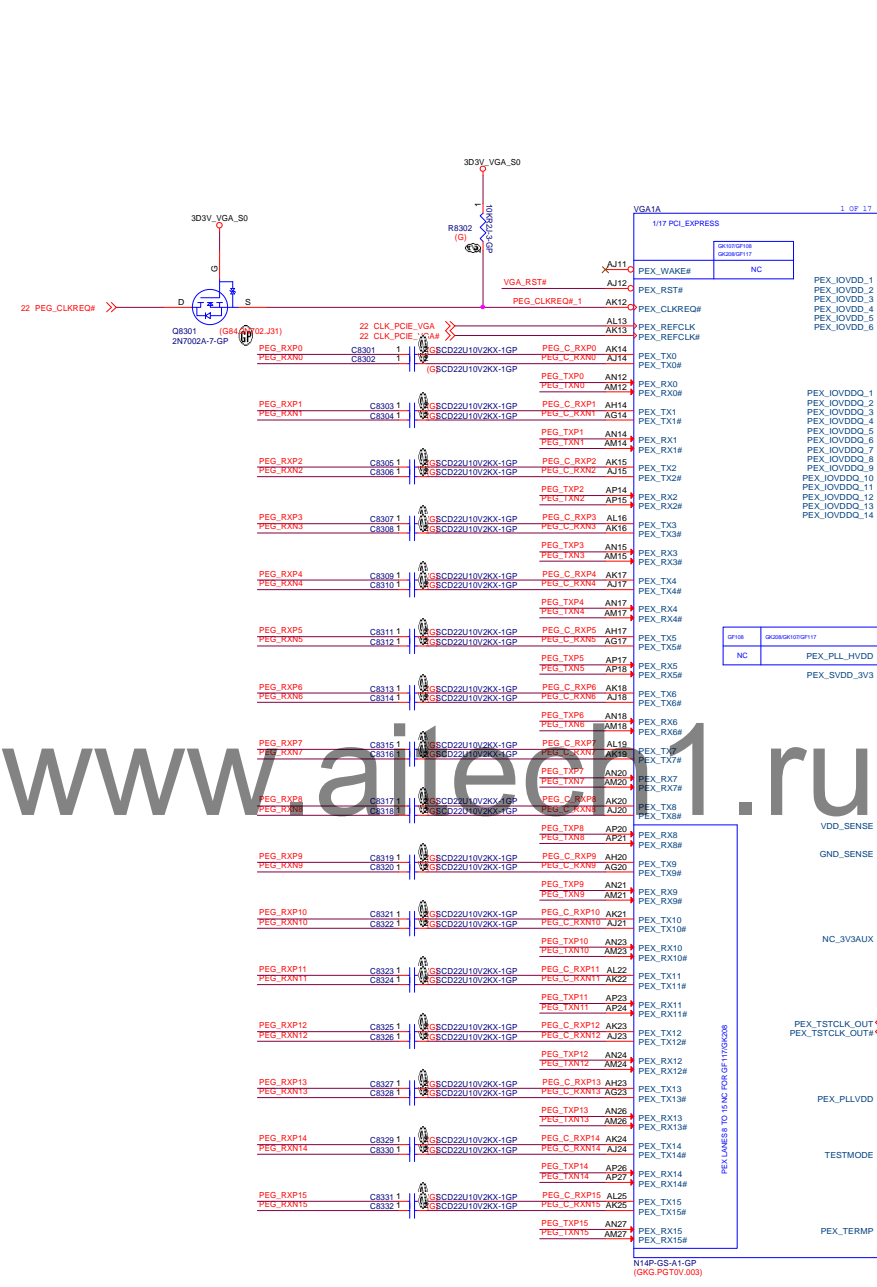
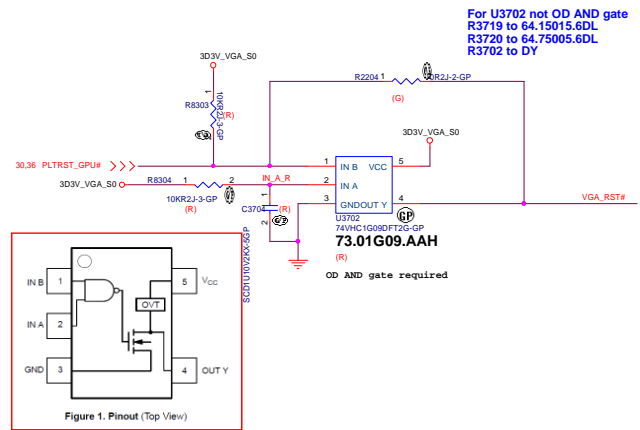
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>PWR BT/Side Key/LED</i>			
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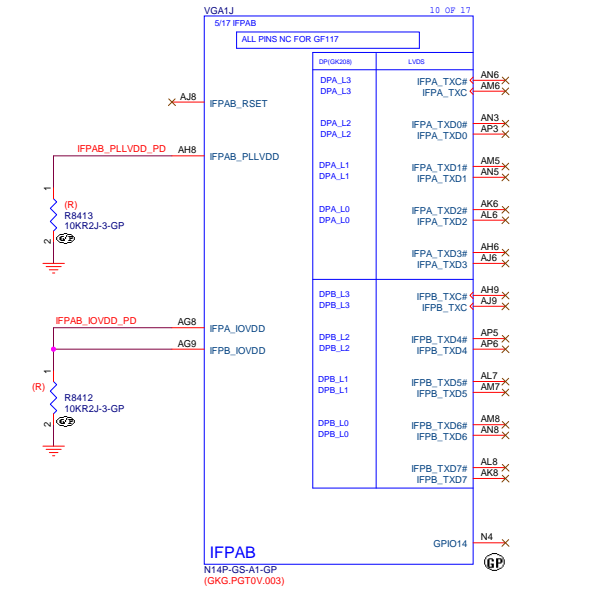
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Title			
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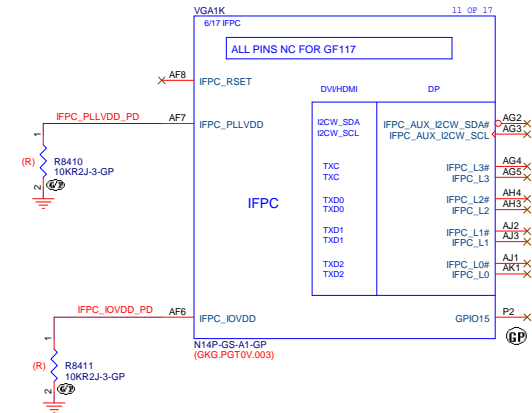


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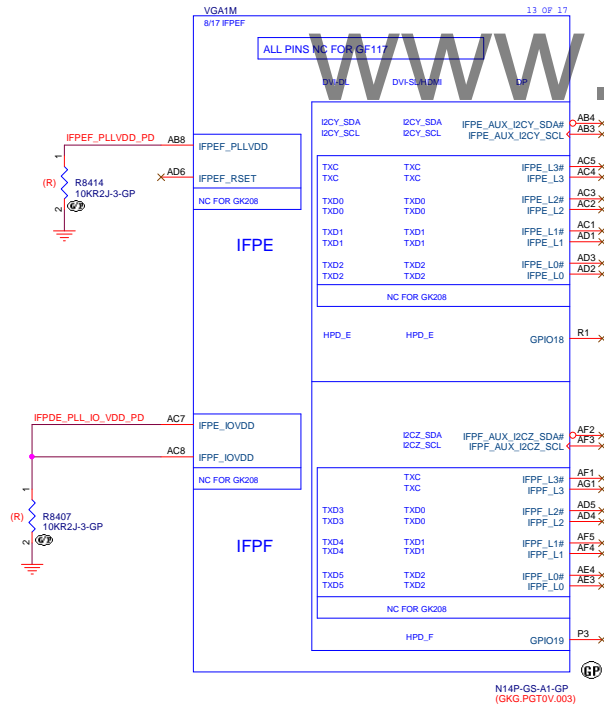
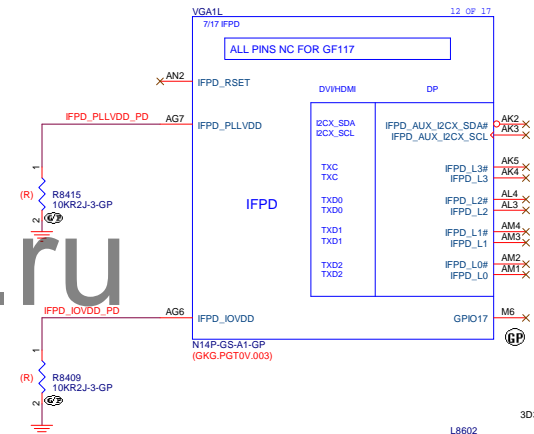
LVDS Interface



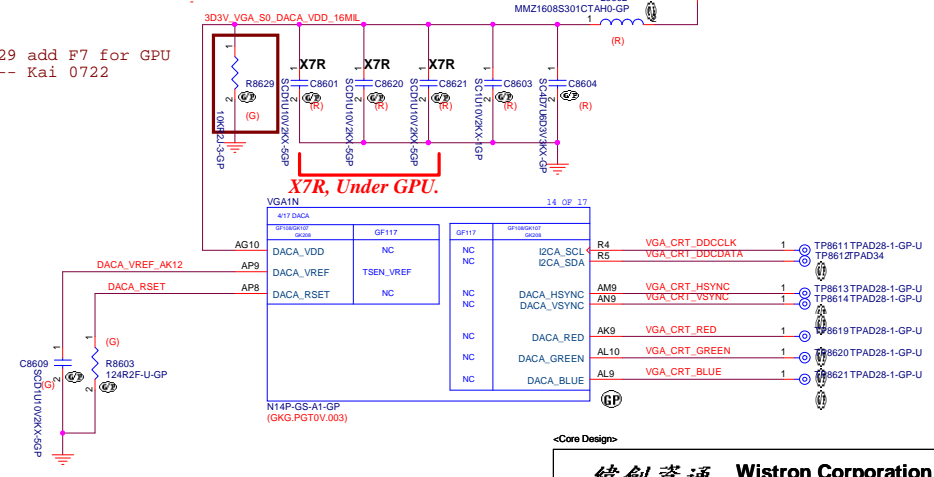
HDMI Interface



EDP Interface



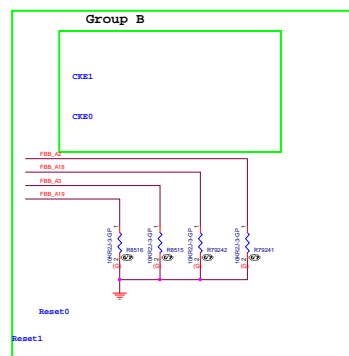
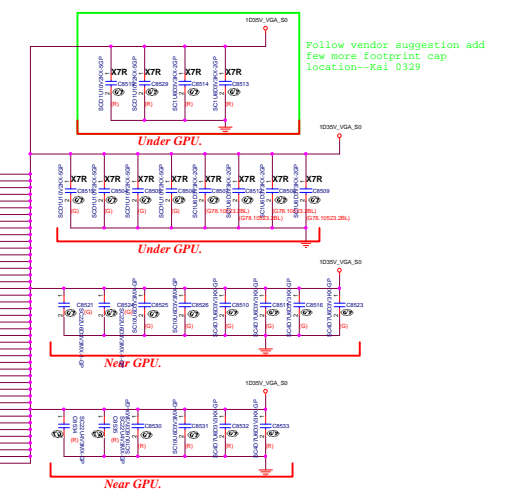
R8629 add F7 for GPU use-- Kai 0722



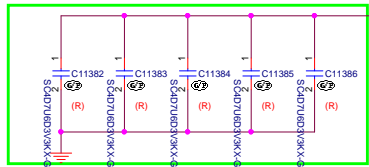
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Taipei Hsien 221, Taiwan, R.O.C.

Title GPU DIGITALOUT(2/5)
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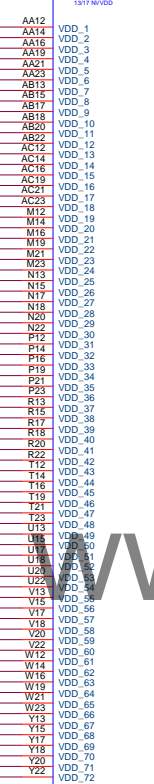


Under GPU 4.7uFx5



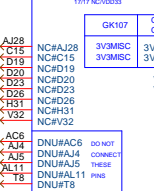
EDP 50A
(TDP 37W)

VGA1F 6 OF 17



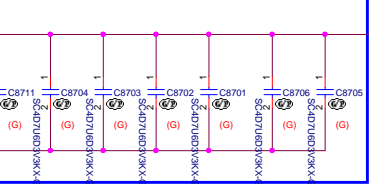
N14P-GS-A1-GP
(GKG.PGT0V.003)

VGA1E 5 OF 17

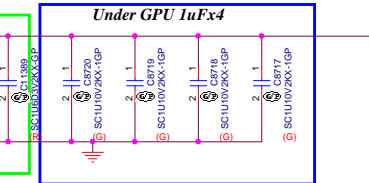


N14P-GS-A1-GP
(GKG.PGT0V.003)

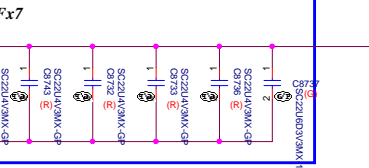
Under GPU 4.7uFx10



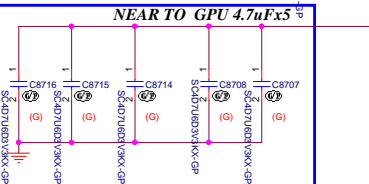
Under GPU 1uFx4



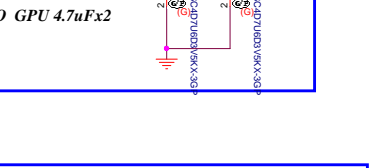
NEAR TO GPU 22uFx7



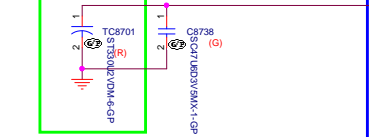
NEAR TO GPU 4.7uFx5



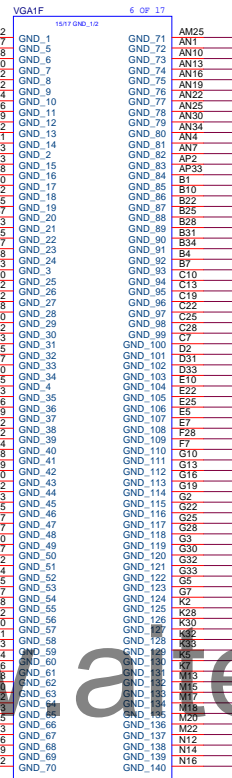
NEAR TO GPU 4.7uFx2



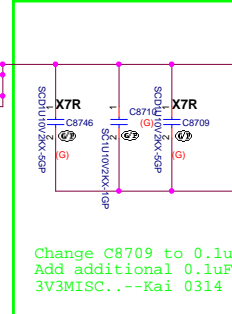
NEAR TO GPU
47uF x1
330uF x1



TC8701 from 470uF to 330uF--Kai 0402



N14P-GS-A1-GP
(GKG.PGT0V.003)

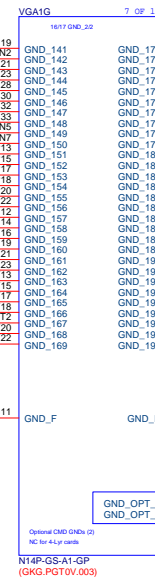


Change C8709 to 0.1uF,
Add additional 0.1uF at
3V3MISC.--Kai 0314

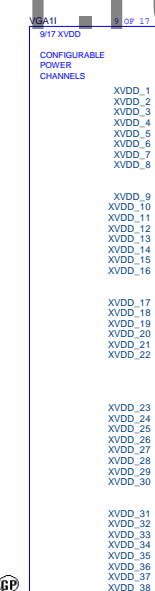
0.1U Under GPU

4.7U NEAR TO GPU

1U NEAR TO GPU



N14P-GS-A1-GP
(GKG.PGT0V.003)

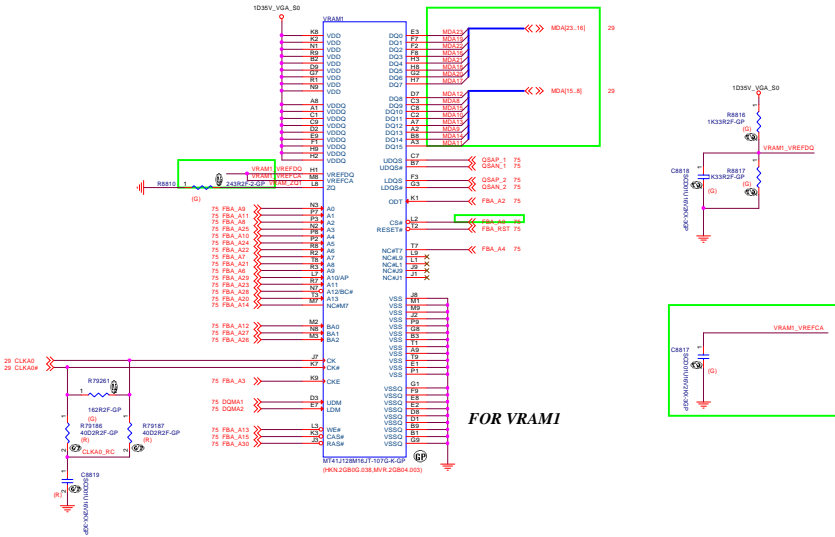


N14P-GS-A1-GP
(GKG.PGT0V.003)

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taichung Hsien 221, Taiwan, R.O.C.

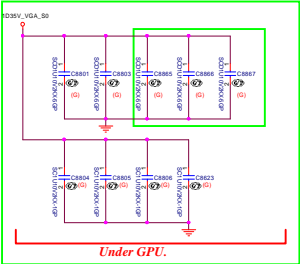
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Size	Document Number	Rev
Custom	PIM86L-Florence	1
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CHANNEL A:Normal Type



VRAM

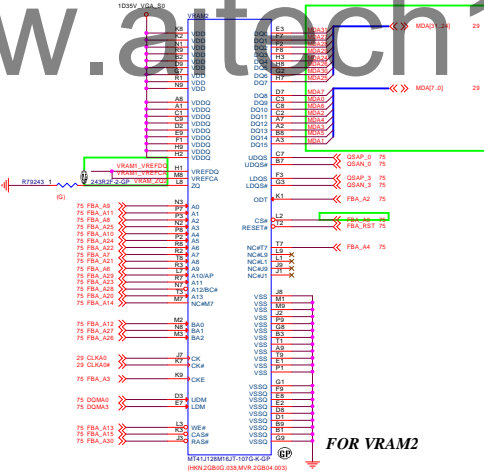
DG requires 5x0.1uF and 2x1.0uF and 1x10uF per VRAM chip



Add VRAM decoupling cap--Kai 0315
Add VRAM decoupling cap--Kai 0329

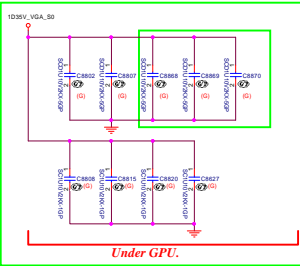
CHANNEL A:Mirrored Type

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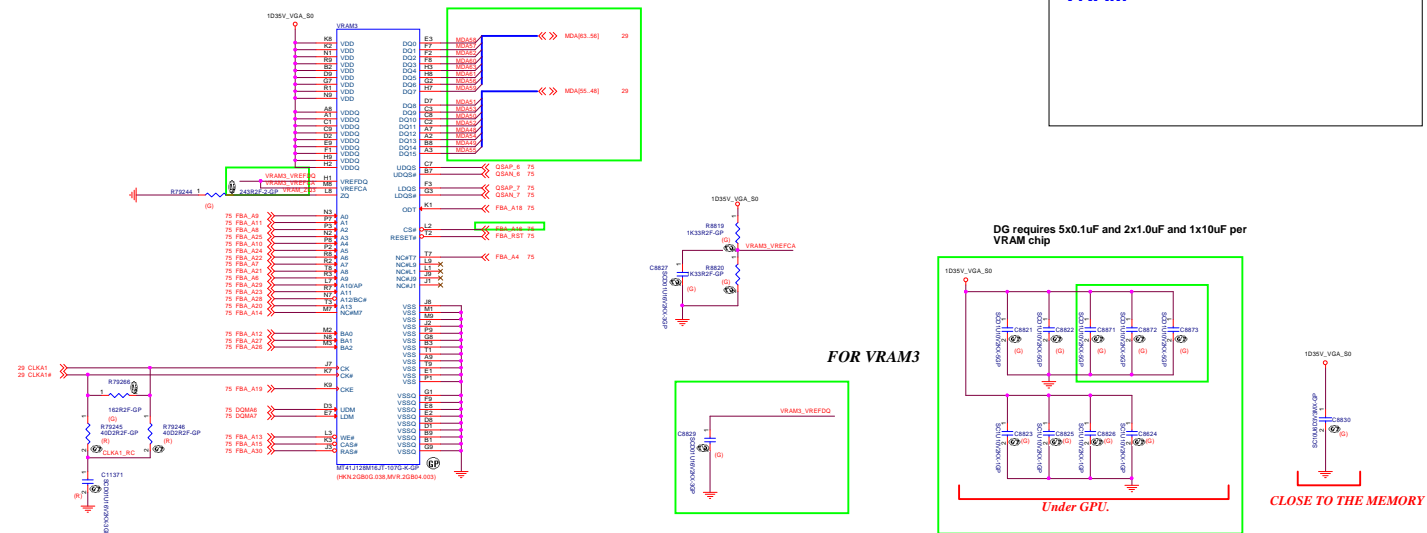
VRAM

DG requires 5x0.1uF and 2x1.0uF and 1x10uF per VRAM chip



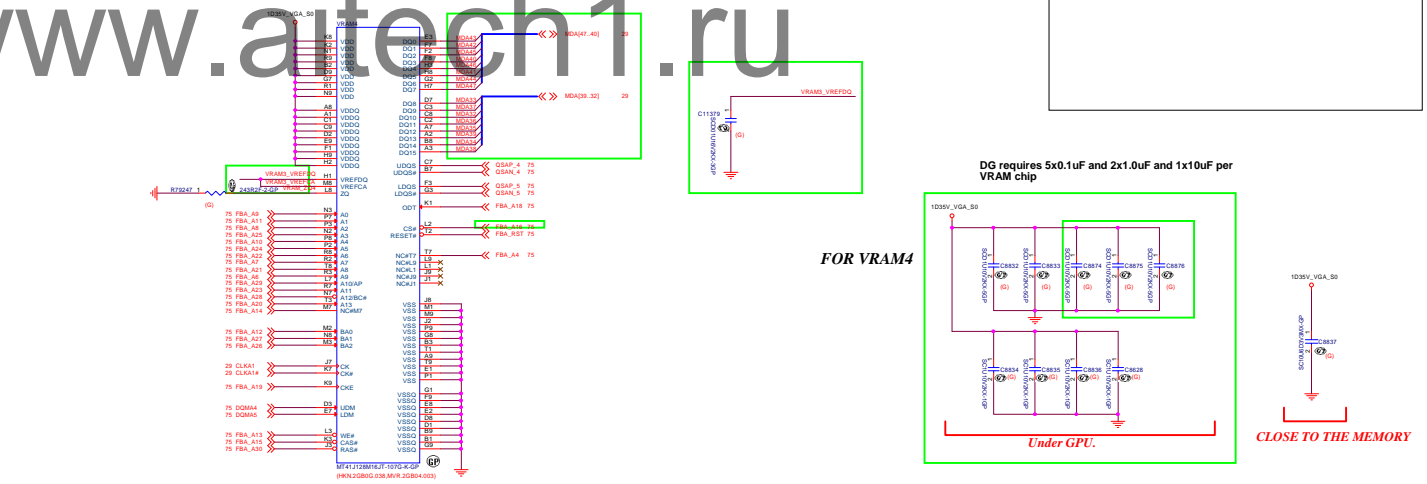
CLOSE TO THE MEMORY

CHANNEL A:Normal Type

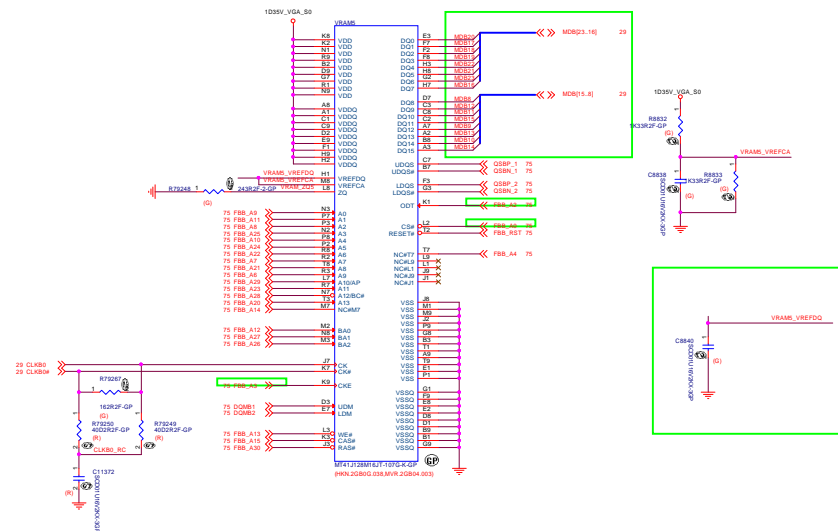


CHANNEL A:Mirrored Type

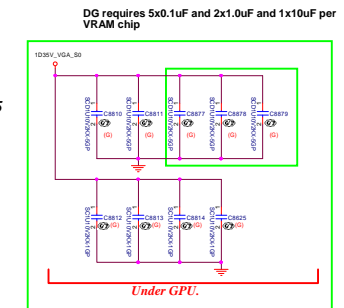
www.aitech1.ru



VRAM



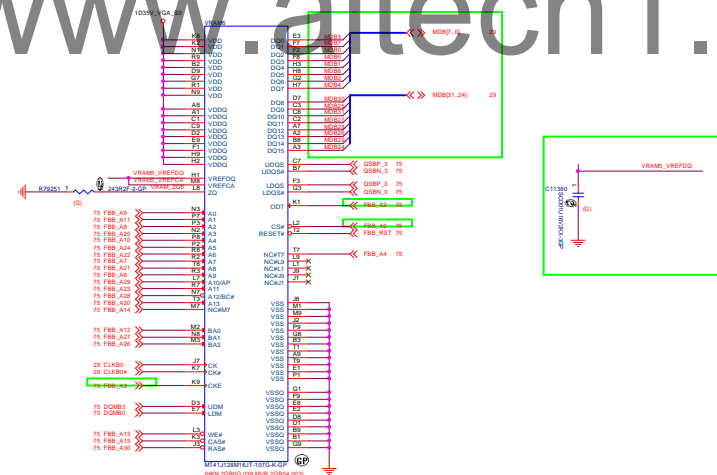
FOR VRAM5



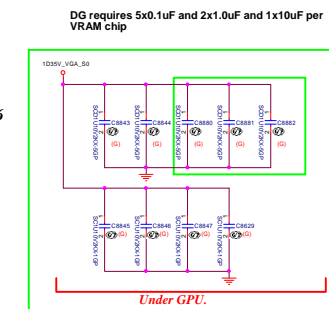
CLOSE TO THE MEMORY

CHANNEL B:Mirrored Type

VRAM

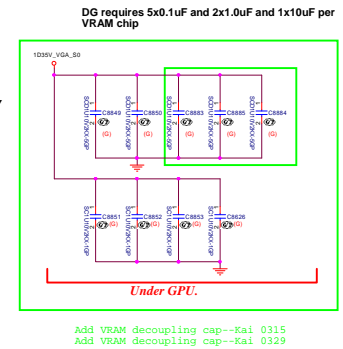


FOR VRAM6

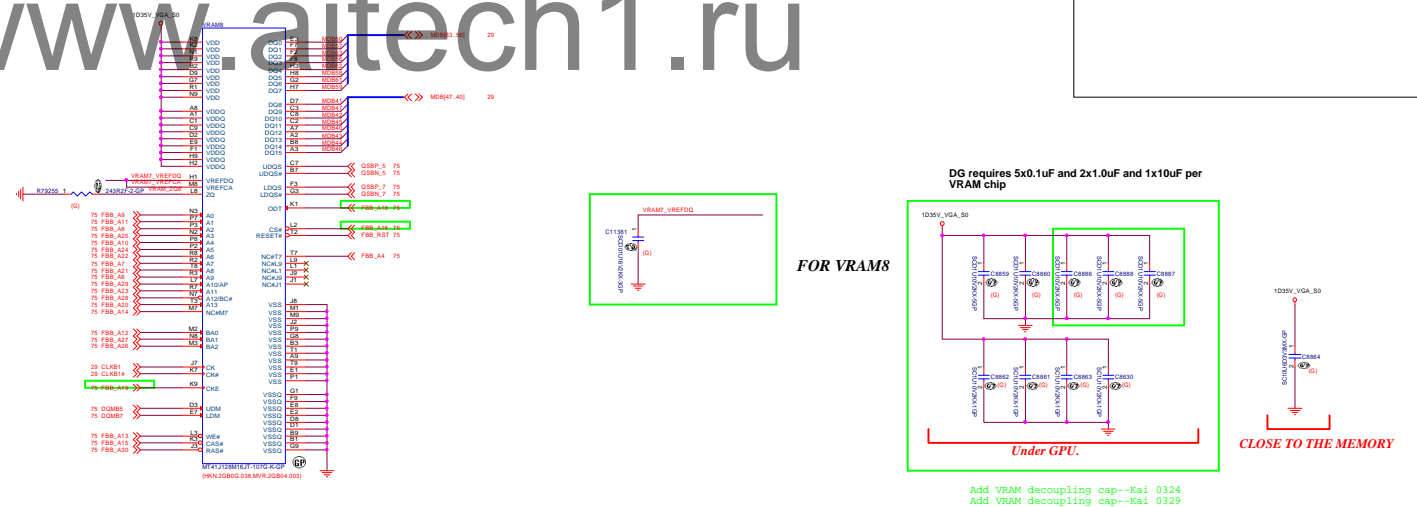
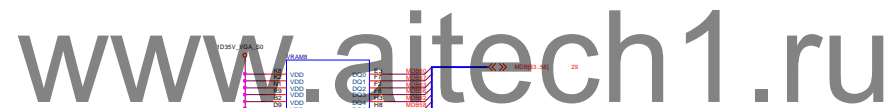


CLOSE TO THE MEMORY

VRAM



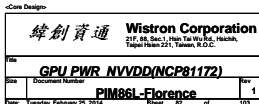
VRAM



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PWM-VID Spec		Config A	Config B	Config C
Vmin	V	0.6	0.6	0.65
Vmax	V	1.2	1.2	1.15
Vboot	V	0.875	0.9	0.9
Voltage Step Vstep	mV	6.25	6.25	25
Number of Voltage Levels N	level	96	96	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676
PWM Minimum Pulse Width T_{ONMIN}	ns	9.26	9.26	74
VID Transient Time T	us	<100	<100	<100
Component Value				
R1 (1%)	K Ω	89	20	39
R2 (1%)	K Ω	39	20	30
R3 (1%)	K Ω	1.5	2	3
R4 (1%)	K Ω	30	18	24
R5 (1%)	K Ω	1.5	0	3
C	nF	1.5	2.7	1.8

PWM-VID Spec		Config A	Config B	Config C
Vmin	V	0.6	0.6	0.65
Vmax	V	1.2	1.2	1.15
Vboot	V	0.875	0.9	0.9
Voltage Step Vstep	mV	6.25	6.25	25
Number of Voltage Levels N	level	96	96	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676
PWM Minimum Pulse Width T_{ONMIN}	ns	9.26	9.26	74
VID Transient Time T	us	<100	<100	<100
Component Value				
R1 (1%)	K Ω	89	20	39
R2 (1%)	K Ω	39	20	30
R3 (1%)	K Ω	1.5	2	3
R4 (1%)	K Ω	30	18	24
R5 (1%)	K Ω	1.5	0	3
C	nF	1.5	2.7	1.8



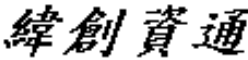
www.aitech1.ru

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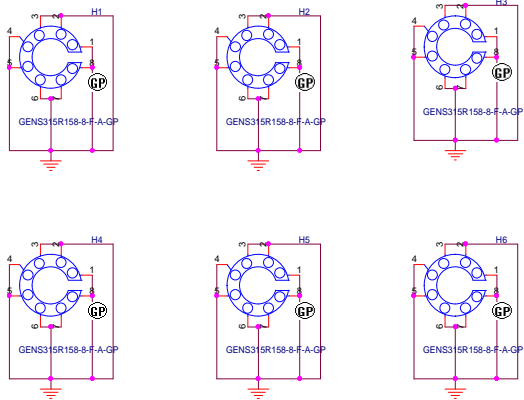
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Title			
<div>PWR BT/Side Key/LED</div>			
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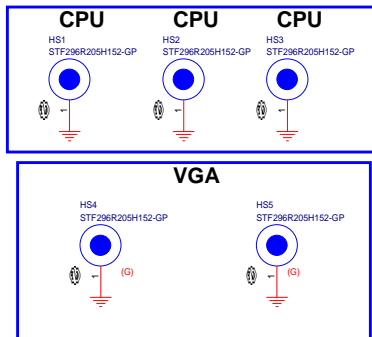
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Title PWR BT/Side Key/LED			
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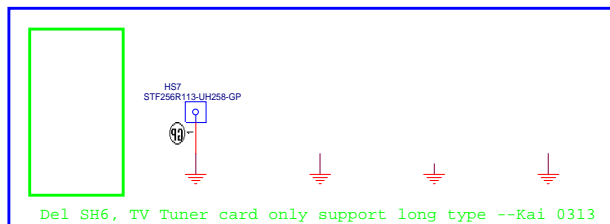
Stand off&Hole



34.3KF01.001 for 5.2mm slot 62.10043.G11
34.3HJ03.001 for 9.0mm slot 62.10043.E41



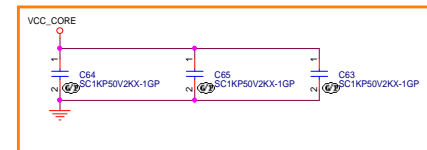
2011/10/7 Add the stand off hole Done



Del SH6, TV Tuner card only support long type --Kai 0313

EMI CAP

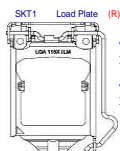
For EMC--Kai 0515



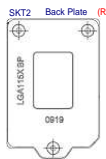
DUMMY BOM

Material part

LGA115x CPU SOCKET Symbol



Vendor: LOTES
P/N: 22.78003.011
Vendor: FOXCONN
P/N: 22.78006.001

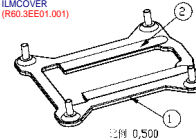


Vendor: LOTES
P/N: 22.78002.011
Thickness: max 2.2mm (含mylar及螺孔高)
Vendor: FOXCONN
P/N: 22.78006.011
Thickness: 2.0mm (含mylar)



Vendor: LOTES
P/N: 22.78005.171
Vendor: FOXCONN
P/N: 22.78005.161

SKT4 ILMCOVER (R60.3EE01.001)



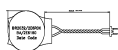
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P/N: 22.78005.171
Vendor: FOXCONN
P/N: 22.78005.161

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Battery Symbol

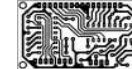


BAT3
BATTERY CR2032
(23.20068.001)
Vendor
P/N:
23.20068.001
23.20023.311
23.22063.001



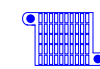
BAT2
BATTERY BR2032_60MM
(R23.24220.612)
Wire Length: 60mm
耐高溫>85C
Vendor
P/N:
23.21208.061
23.24220.612

PCB Symbol

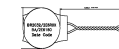


PCB1
PCB
(R)

Del PCHHS1 by Thermal--Ryan 0225
Heatsink Symbol



PCHHS1
HEATSINK
(R60.3MN01.001)
Vendor
P/N:
60.3MN01.011(second source)
60.3MN01.001



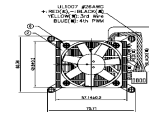
BAT1
BATTERY CR2032_30MM
(R23.21221.024)
Wire Length: 30mm
Vendor
P/N:
23.21221.024
23.21212.031

LABEL



MB serial NO# and MAC address
45.41101.001 -> 35 x 15mm (DEL)
40.3KP03.001 -> 35 x 15mm (耐高溫)
45.41107.011 -> 70 x 8mm
45.41115.001 -> 34 x 13.5mm

Heatsink+FAN Symbol



HSFAN1
(R60.3KN01.001)

Vendor
P/N:

<Core Design>

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File	Document Number	Rev
Stand off&Hole&EMI Cap&DUMMY BOM	PIM86L-Florence	1
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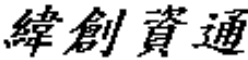
www.aitech1.ru

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Title			
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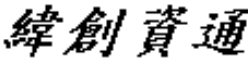
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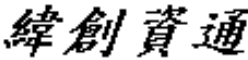
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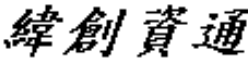
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Title <i>PWR BT/Side Key/LED</i>			
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<Core Design>

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<i>PWR BT/Side Key/LED</i>			
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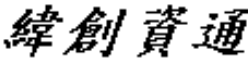
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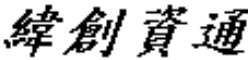
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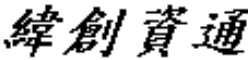
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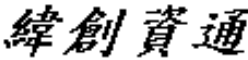
www.aitech1.ru

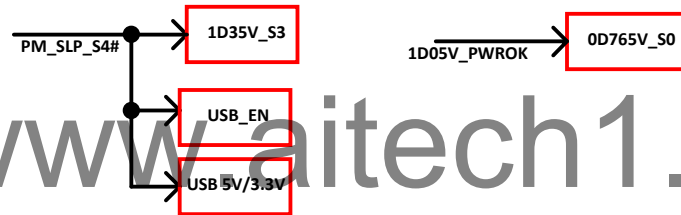
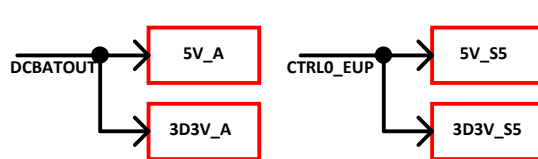
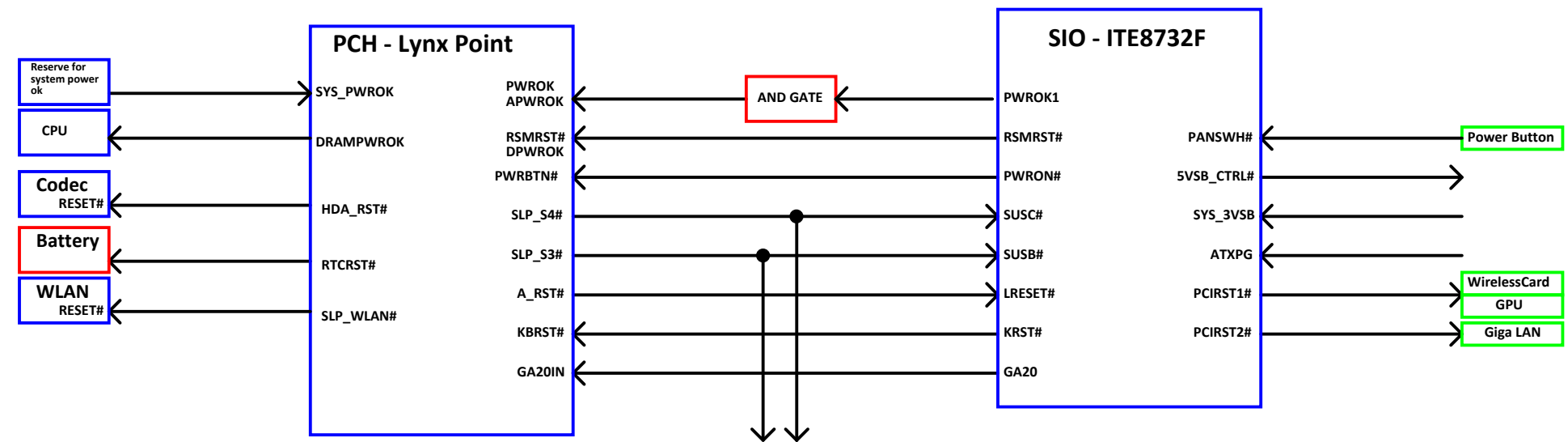
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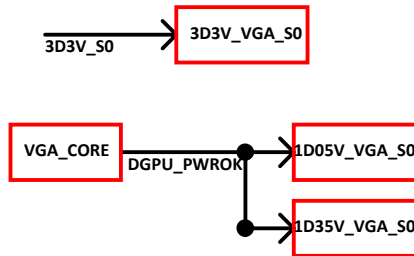
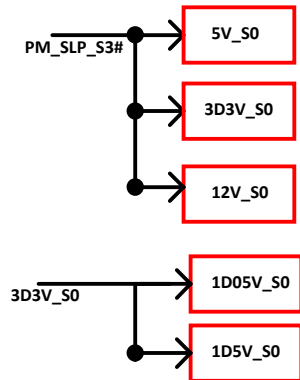
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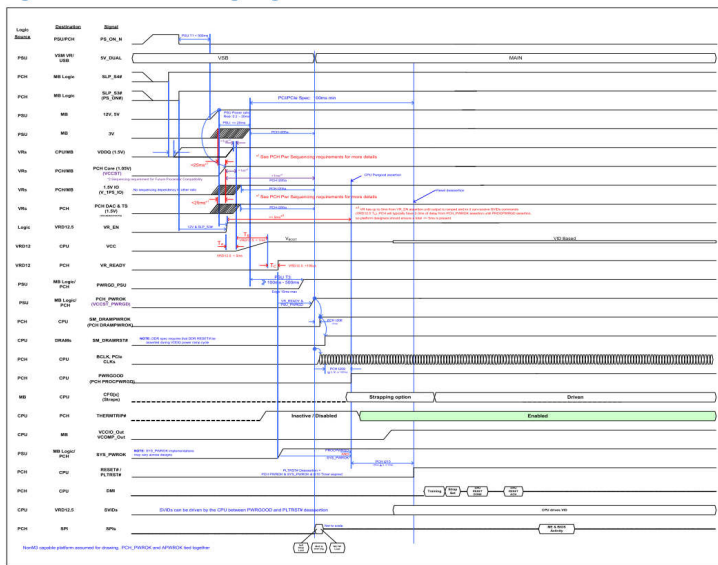


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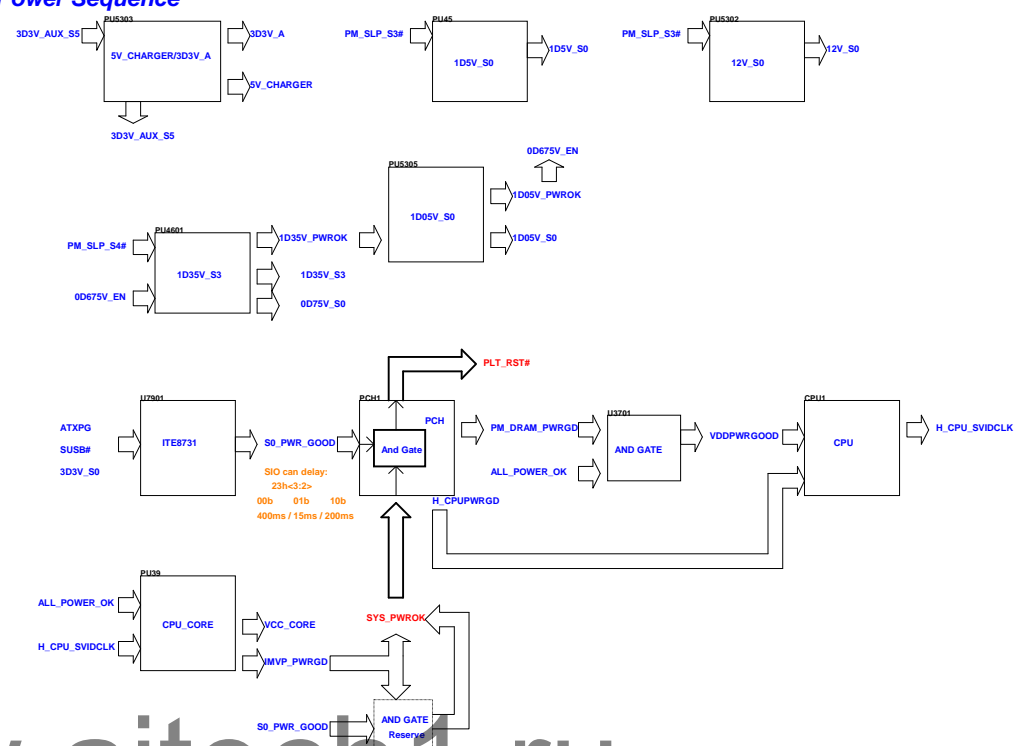


System sequence

Figure 36-3. Platform Timing Diagram - POR

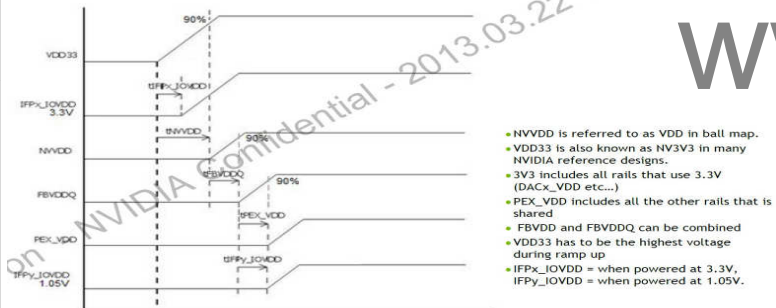


Power Sequence



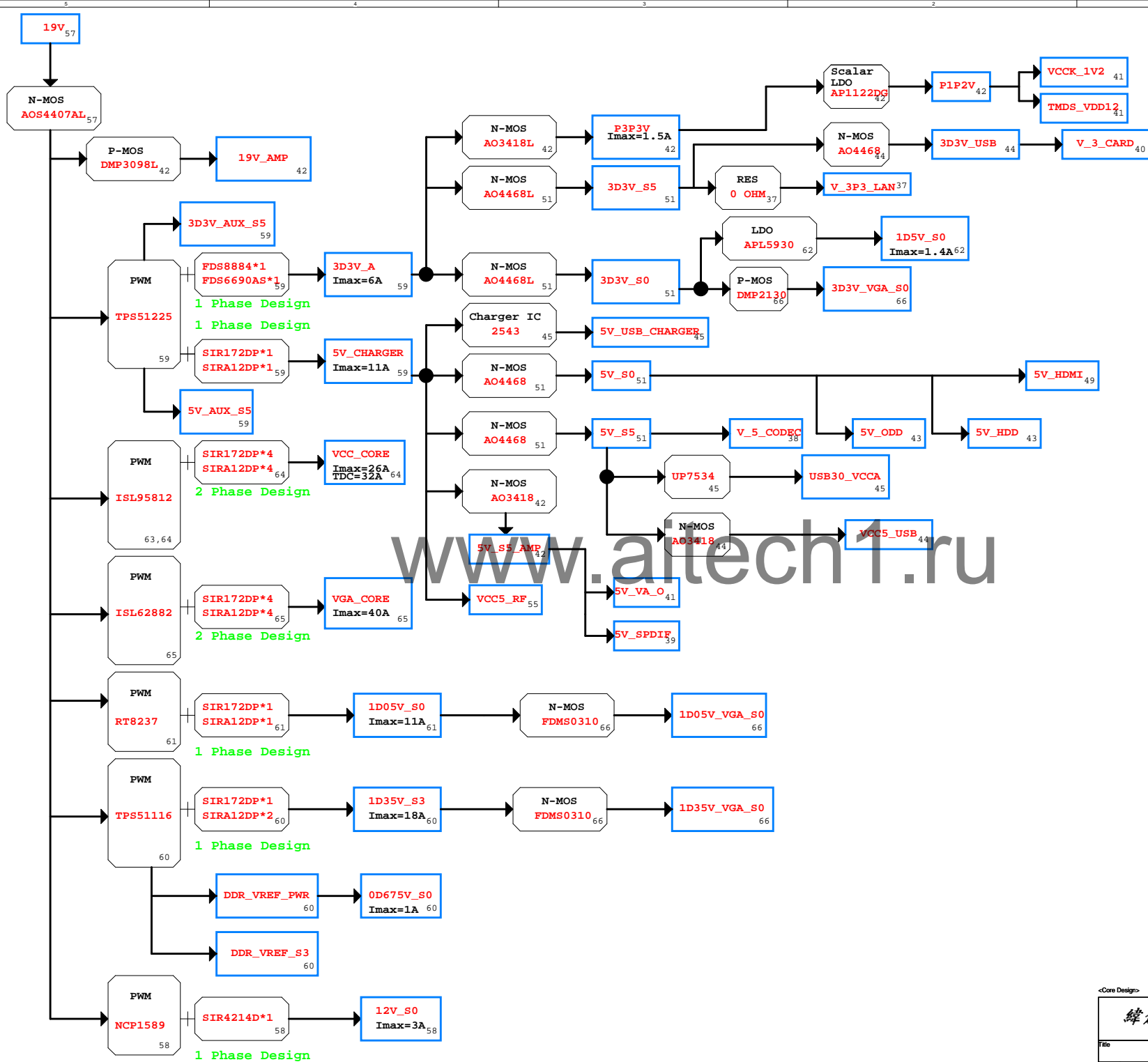
GPU sequence

In GC6 mode, all of the power rails are down except for FBVDDQ (see section 3.5, *GC6 Power Saving State* starting on page 53).



- NVVDD is referred to as VDD in ball map.
- VDD33 is also known as NV3V3 in many NVIDIA reference designs.
- 3V3 includes all rails that use 3.3V (DAXx_VDD etc...)
- PEX_VDD includes all the other rails that is shared
- FBVDD and FBVDDQ can be combined
- VDD33 has to be the highest voltage during ramp up
- IFPx_I0VDD = when powered at 3.3V, IFPy_I0VDD = when powered at 1.05V.

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POWER DELIVERY CHART			
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PCH GPIO table

GPIO	IC PIN NAME	Power Well	Default	Level Default	Signal Name	Usage	BIOS Programming					Comment
							S0	S1	S3	S4	S5	
GPIO0	BA_BUSTV	Core	GPI	Low	PCH_GPIO0	No	GPIOH	GPIOH	DM	DM	DM	
GPIO1	TACH1	Core	GPI	Low	EC_SMIW	EC_SMIW	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO2	PIRQ0#	Core	GPI	Low	INT_FIRQ0#	No	GPIOH	GPIOH	DM	DM	DM	
GPIO3	PIRQ#	Core	GPI	Low	INT_FIRQ#	No	GPIOH	GPIOH	DM	DM	DM	
GPIO4	PIRQ0#	Core	GPI	Low	INT_FIRQ0#	No	GPIOH	GPIOH	DM	DM	DM	
GPIO5	PIRQ#	Core	GPI	Low	INT_FIRQ#	No	GPIOH	GPIOH	DM	DM	DM	
GPIO6	TACH2	Core	GPI	Low	DDPU_HPD_INTR#	DDPU_HPD_INTR#	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO7	TACH3	Core	GPI	Low	TV_DISABLE#	Low: TV Tuner disable High: TV Tuner enable	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO8	-	Sus	GPO	High	PCH_GPIO8	No	GPIOL	GPIOL	DM	DM	DM	refer to Sabina GPIO 8 : GPIO_L
GPIO9	OC0#	Sus	Native	Low	mSATA_DET#	Low: M-SATA disable High: M-SATA Tuner enable	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO10	OC0#	Sus	Native	Low	Wake_FICIE	Low: NA High: Wake FICIE	DM	DM	DM	DM	DM	
GPIO11	SMBALERT#	Sus	Native	Low	LPC_PMR#	No	GPIOH	GPIOH	GPIOH	DM	DM	
GPIO12	LAN_PHY_F_WL_CTL#	DSW	Native	Low	USB_CHARGER_WAKE#	USB_CHARGER_WAKE#	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO13	-	Sus	GPI	Low	SPU_WF_R_N	High-WP Low: NA	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO14	OC7#	Sus	Native	Low	Wake_LDM	Low: NA High: Wake FICIE	DM	DM	DM	DM	DM	
GPIO15	-	Sus	GPO	Low	LAN_EN_FWR	Low: Enable High: Disable	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO16	SATA0SP	Core	GPI	Low	SATA0SP	No	GPI	GPI	GPI	GPI	GPI	
GPIO17	TACH0	Core	GPI	High	DDPU_FIRQ0#	DDPU_FIRQ0#	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO18	POICLKIRQ1#	Core	Native	High	PCH_CLK_PCIE#SATA_REQ#	No	GPI	GPI	DM	DM	DM	
GPIO19	SATA1SP	Core	GPI	High	SATA1SP	Steering Pin	GPI	GPI	DM	DM	DM	
GPIO20	POICLKIRQ2#	Core	Native	High	PCH_CLK_PCIE#	No	Native	Native	Native	Native	Native	
GPIO21	SATA2SP	Core	GPI	High	SATA2SP	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO22	SLOC0#	Core	GPI	High	PCH_GPIO22	High: UAA_VRAM800MHz Low: VDRAM800MHz	GPI	GPI	GPI	GPI	GPI	
GPIO23	SDOR#	Core	Native	High	NO	DM	DM	DM	DM	DM	DM	
GPIO24	-	Sus	GPO	Low	NO	DM	DM	DM	DM	DM	DM	
GPIO25	POICLKIRQ3#	Core	Native	High	CLK_PCIE_WLAN_REQ#	WLAN REQ	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO26	POICLKIRQ4#	Sus	Native	Low	ME_CNTL	Low/Normal High: ME disable	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO27	-	DSW	GPI	Low	PCH_GPIO27	No	GPI	GPI	GPI	GPI	GPI	
GPIO28	-	Sus	GPO	Low	PCH_GPIO28	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO29	SLP_LAN#	DSW	Native	Low	PCH_SLP_WLAN_N	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO30	SUS_PWR_ACK	Sus	Native	Low	SUS_PWR_ACK	SUS_PWR_ACK	Native	Native	Native	Native	Native	
GPIO31	AC_PRESENT	DSW	GPI	Low	AC_PRESENT	No	GPIOL	GPIOL	GPIOL	GPIOL	GPIOL	
GPIO32	Quirk (Mobile Only) / GPIO32 (Desktop Only)	Core	GPO	High	NA	NA	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO33	DOCK0#	Core	GPO	High	PCH_GPIO33	Steering Pin	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO34	-	Core	GPI	High	GPIO34	NA	GPIOL	GPIOL	GPIOL	GPIOL	GPIOL	
GPIO35	MM#	Core	GPO	Low	PP_DET#	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO36	SATA2SP	Core	GPI	Low	SATA2SP	Steering Pin	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO37	SATA2SP	Core	GPI	Low	SATA2SP	Steering Pin	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO38	SLOC0	Core	GPI	Low	SPU_HPD_C	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO39	SATA0UT0	Core	GPI	Low	GPI_CBL_DET	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO40	OC1#	Sus	Native	Low	OC_2#	UBC OC2# event	Native	Native	Native	Native	Native	
GPIO41	OC2#	Sus	Native	Low	W3_DISABLE_N	Low-WLBT disable High-WLBT enable	Native	Native	Native	Native	Native	
GPIO42	OC3#	Sus	Native	Low	W1_DISABLE_N	Low-WLBT disable High-WLBT enable	Native	Native	Native	Native	Native	
GPIO43	OC4#	Sus	Native	Low	USB_OC_01#_N	UBC OC1# event	Native	Native	Native	Native	Native	
GPIO44	POICLKIRQ5#	Sus	Native	Low	PCH_CLK_LAN_REQ#	LAN REQ	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO45	POICLKIRQ6#	Sus	Native	Low	PCH_CLK_REQ#	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO46	POICLKIRQ7#	Sus	Native	Low	EDID_RDY	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO48	SATA0UT1	Core	GPI	Low	KEY1_TEST	Test key	GPI	GPI	GPI	GPI	GPI	
GPIO49	SATA0SP	Core	GPI	High	PCH_GPIO49	No	GPI	GPI	GPI	GPI	GPI	
GPIO50	-	Core	GPI	Low	PCH_GPIO50	GPIO	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO51	-	Core	GPO	High	PCH_GPIO51	Steering Pin	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO52	-	Core	GPI	Low	PCH_GPIO52	GPIO	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO53	-	Core	GPO	High	PCH_GPIO53	Steering Pin	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO54	-	Core	GPI	Low	PCH_GPIO54	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO55	PEB_CLKV_O#	Core	GPO	High	PCH_GPIO55	Steering Pin	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO56	-	Sus	Native	High	PEB_CLKV_O#	No	Native	Native	Native	Native	Native	
GPIO57	-	Sus	GPI	Low	USB_PWR_ON	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO58	SMB1QW#	Sus	Native	High	SIO_SCL1	PCH SMBUS to SIO	Native	Native	Native	Native	Native	
GPIO59	OC0#	Sus	Native	Low	USB_OC_01#_N	UBC OC1# event	Native	Native	Native	Native	Native	
GPIO60	SMBALERT	Sus	Native	Low	DRAMRST_CNTRL_PCH	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO61	SUS_STAT#	Sus	Native	High	GPIO61_R	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO62	SUS_CLK	Sus	Native	Low	PCH_SUS_CLK	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO63	SLP_DSW	Sus	Native	High	GPIO63_R	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO64	CLKOUTFILE_X0	Core	Native	Low	NA	NA	Native	Native	Native	Native	Native	
GPIO65	CLKOUTFILE_X1	Core	Native	Low	CLKOUTFILEX1	BA	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO66	CLKOUTFILE_X2	Core	Native	Low	NA	BA	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO67	CLKOUTFILE_X3	Core	Native	Low	NA	BA	GPI	GPI	GPI	GPI	GPI	
GPIO68	TACH4	Core	GPI	Low	SMBUS_ISP	High: Simultaneous Mode Low: Isolate Mode	GPI	GPI	GPI	GPI	GPI	
GPIO69	TACH5	Core	GPI	Low	KEY2_TEST	High: No PS2 cable Low: PS2 released	GPI	GPI	GPI	GPI	GPI	
GPIO70	TACH6	Core	Native	High	KEY0_TEST	No	GPI	GPI	GPI	GPI	GPI	
GPIO71	TACH7	Core	Native	High	PANEL_OFF_R	No	GPI	GPI	GPI	GPI	GPI	
GPIO72	BATLOW#	DSW	Native	Low	BATLOW#	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO73	POICLKIRQ8#	Sus	Native	Low	PCH_CLK_TV_REQ#	No	GPIOL	GPIOL	GPIOH	GPIOH	GPIOH	
GPIO74	SMBALERT#	Sus	Native	Low	NO	No	GPIOH	GPIOH	GPIOH	GPIOH	GPIOH	
GPIO75	SMB1QW#	Sus	Native	Low	SIO_SDA1	PCH SMBUS to SIO	Native	Native	Native	Native	Native	

XIO GPIO table

IC Pin Name	Power Well	Default	Signal Name	Usage	BIOS Programming						Comment
					Output Type	S0	S1	S3	S4	S5	
PCIRSTM/ GPIO10	Suspend	Native	SIO_CIRRX1_R	SIO_CIRRX1_R	NA						BIOS will set this pin to IR Function
PCIRSTM/ GPIO11	Suspend	Native	PCIRST2#	PCIRST	Push Pull						
PCIRSTM/ GPIO12	Suspend	Native	PCIRST1#	PCIRST	Push Pull						
PWROK1/ GPIO13	Suspend	Native	PWROK3_1	PWROK3	Open Drain						
VCORE_EN/PCH_C1/ GPIO14	Suspend	Native	SMML_CLK	SMML_CLK	Open Drain						
PCIRSTNM/ CIRTX2/ GPIO15/ CPU_PG	Suspend	Native	SIO_PCIRSTNM	PCIRST							
SVSR_CTLR#/ CIRX2/ GPIO16	Suspend	Native	NA	NA	NA						
R12#/ GPIO17	Suspend	Native	NA	NA	NA						
CT32M/ GPIO20	Suspend	Native	LIM_SEL	USB CHARGER	Open Drain	GPO/High	GPO/High	GPO/High	GPO/High	GPO/High	
DCD2M/ GPIO21	Suspend	Native	PANEL_CTRL	not used	Open Drain	GPO/High	GPO/High	GPO/High	GPO/High	GPO/High	Display On/Off
SC0/ GPIO22	Suspend	Native	SIO_SCK_R	EEPROM							
SJ/ GPIO23	Suspend	Native	SIO_SJ	EEPROM							
RTS2M/ GPIO24	Suspend	Native	PWRBTN_IN_C	RP_PWRBTN	NA						
DSR2M/ GPIO25	Suspend	Native	PCIE_WLAN_WAKE#	not used	Open Drain						
SOULT/ GPIO26	Suspend	Native	SIO_UART1_TX	UART1_TX							
SN2/ GPIO27	Suspend	Native	SIO_UART1_RX	UART1_RX							
ATXPG/ GPIO30	Suspend	Native	SIO_ATXPG	SIO_ATXPG							
PWMOUT/ GPIO31	Suspend	Native	NA	NA	Open Drain						
DPWROK/ GPIO32	Suspend	Native	NA	NA	NA						
SUSACKR/ GPIO33	Suspend	Native	CTRLD	EUP function	NA	GPO/High	GPO/High	GPO/High	GPO/High	GPO/High	
SUSWAKW/ GPIO34	Suspend	Native	USB_CHARGER_CTL3	USB CHARGER	Open Drain	GPO/High	GPO/High	GPO/High	GPO/High	GPO/High	
FAM_TAC4/ GPIO35	Suspend	Native	USB_CHARGER_CTL1	USB CHARGER	Open Drain	GPO/High	GPO/High	GPO/High	GPO/High	GPO/High	
FAM_CTL3/ GPIO36	Suspend	Native	AMP_PDN#	AMP_Mute	NA						Please Follow Pisa
FAM_TAC3/ GPIO37	Suspend	Native	EC_AMP_RST	AMP_Rst	NA						Please Follow Pisa
SVSRSW/ GPIO40	Suspend	Native	PM_SLP_S3M_3	PM_SLP_S3	Open Drain	GPI	GPI	GPI	GPI	GPI	
PWROK2/ GPIO41	Suspend	Native	PWROK3_2	PWROK3							
PS0NM/ GPIO42	Suspend	Native	SIO_PS0N_N	SIO_PS0N							
PANSWHM/ GPIO43	Suspend	Native	PB_IN_N_1	PB_IN_N							
PWR0NM/ GPIO44	Suspend	Native	SW_ON_N_SIO	SW_ON_N							
D_1X0/ SMCCLK2/ GPIO46	Suspend	GPIO	SMBCLK2_SIO	For AMP used	Open Drain						
D_1X0/ SMDAT2/ GPIO47	Suspend	GPIO	SMBDAT2_SIO	For AMP used	NA						
SIO/ GPIO50	Suspend	Native	SIO_S0	EEPROM	Push Pull						
FAM_CTL2/ GPIO51	Suspend	Native	SUSLED_3_N	SUS LED	Open Drain	GPO/H	GPO/H	GPO/L	GPO/H	GPO/H	
FAM_TAC2/ GPIO52	Suspend	Native	EC_SMI#	OSD LINK with PCH	Open Drain	GPO/H	GPO/H	GPO/H	GPO/H	GPO/H	
SUSC/ GPIO53	Suspend	Native	PM_SLP_S4_N	PM_SLP_S4_N	Open Drain	GPI	GPI	GPI	GPI	GPI	
PMBW/ GPIO54	Suspend	Native	LPC_PMB#	LPC_PMB#							
RSARSTW/ CIRX1/ GPIO55	Suspend	Native	ICH_SMRST_N_R	ICH_SMRST							
MCLK/ GPIO56	Suspend	Native	MCLK	MCLK							
MDAT/ GPIO57	Suspend	Native	MDAT	MDAT							
KCLK/ GPIO60	Suspend	Native	KBCLK	KBCLK							
KDAT/ GPIO61	Suspend	Native	KDAT	KDAT							
KRSTW/ GPIO62	Suspend	Native	H_RCIN#	H_RCIN#	Push Pull	NA	NA	NA	NA	NA	
SLP_SUSV/ IOT_EN/ GPIO63	Suspend	Native	NA	NA	Open Drain	NA	NA	NA	NA	NA	
GPIO70/KSIO	Suspend	GPIO	DET_HDMI	DET_HDMI_IN	Open Drain	GPI/Low	GPI/Low	GPI/Low	GPI/Low	GPI/Low	
GPIO71/KS1	Suspend	GPIO	SCALAR_IN	CTRL SCALAR POWER	Open Drain	GPO/High	GPO/High	GPO/High	GPO/High	GPO/High	
GPIO72/KS00	Suspend	GPIO	EUP_DSW_SEL	EUP_DSW_SEL	Open Drain	GPI	GPI	GPI	GPI	GPI	
GPIO73/KS01	Suspend	GPIO	SIO_PANEL_ON	PANEL_ON	Open Drain	GPO/High	GPO/High	GPO/High	GPO/High	GPO/High	
GPIO74/KS02	Suspend	GPIO	SIO_PANEL_OFF	PANEL_OFF	Open Drain	GPO/High	GPO/High	GPO/High	GPO/High	GPO/High	
GPIO75/KS04	Suspend	GPIO	SIO_SIOV	Not used	Open Drain	GPO/High	GPO/High	GPO/High	GPO/High	GPO/High	
GPIO76/KS05	Suspend	GPIO	PATBUS_SIO	PATBUS_SIO	Open Drain	GPO/High	GPO/High	GPO/High	GPO/High	GPO/High	
GPIO77/KS05	Suspend	GPIO	PEL_WLAN_WAKE#	WLAN_WAKE#	Push Pull	GPO/High	GPO/High	GPO/High	GPO/High	GPO/High	
GPIO78/SMLCK0	Suspend	GPIO	TP_SIO_SMBCLK0	NA	NA						
GPIO79/SMLCK0	Suspend	Native	TP_SIO_SMBDAT0	NA	Open Drain	GPI/High	GPI/High	GPI/High	GPI/High	GPI/High	

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2/F, 4th, 5th, 11th, 12th, 13th, 14th, 15th, 16th, 17th, 18th, 19th, 20th, 21st, 22nd, 23rd, 24th, 25th, 26th, 27th, 28th, 29th, 30th, 31st, 32nd, 33rd, 34th, 35th, 36th, 37th, 38th, 39th, 40th, 41st, 42nd, 43rd, 44th, 45th, 46th, 47th, 48th, 49th, 50th, 51st, 52nd, 53rd, 54th, 55th

CPU HASWELL

SA CK_N_0
SA CK_P_0
SA CK_N_1
SA CK_P_1

M_A_DIM0_CLK_DDR#0/M_A_DIM0_CLK_DDR0
M_A_DIM0_CLK_DDR#1/M_A_DIM0_CLK_DDR1

DIMM1

SB_CKN0
SB_CK0
SB_CKN1
SB_CK1

M_B_DIM0_CLK_DDR#0/M_B_DIM0_CLK_DDR0
M_B_DIM0_CLK_DDR#1/M_B_DIM0_CLK_DDR1

DIMM2

PCH LYNX POINT(HM86)

CLKIN_DMI_N
CLKIN_DMI_P

CLKOUT_PEG_A_N
CLKOUT_PEG_A_P

100MHz

GPU(SUN_XT)

27MHz

CLKIN_GND_N
CLKIN_GND_P

CLKOUT_PCIE_N_0
CLKOUT_PCIE_P_0

100MHz

TV Tuner

CLKIN_DOT96N
CLKIN_DOT96P

CLKOUT_PCIE_N_3
CLKOUT_PCIE_P_3

100MHz

Mini PCIE WLAN+BT

CLKIN_SATA_N
CLKIN_SATA_P

CLKOUT_PCIE_N_5
CLKOUT_PCIE_P_5

100MHz

LAN RTL8111FA

25MHz

CLKOUT_DMI_N
CLKOUT_DMI_P

100MHz

BCLK

CLKOUT_DP_N
CLKOUT_DP_P

100MHz

SSC_DPLL_REF

CLKOUT_DPNS_N
CLKOUT_DPNS_P

100MHz

DPLL_REF

CLKOUTFLEX1/GPIO65

CLK_48M_SIO

SIO IT8732F

CLKIN(37)

CLKOUT_33MHZ3

CLK_PCI_SIO

PCICLK(47)

HDA_BCLK

PCH_HDA_BITCLK_R/24MHZ

AUDIO ALC269Q

SPI_CLK

24MHz/48MHz/100MHz

SPI ROM

CLKOUT_33MHZ1

33MHz

LPC Debug Port

RTCCCLK

(for Master)
XTAL25_OUT
XTAL25_IN

25MHz

(for RTC)
RTCX1
RTCX2

32.768KHz

SCALAR RTL2487

14.31818MHz

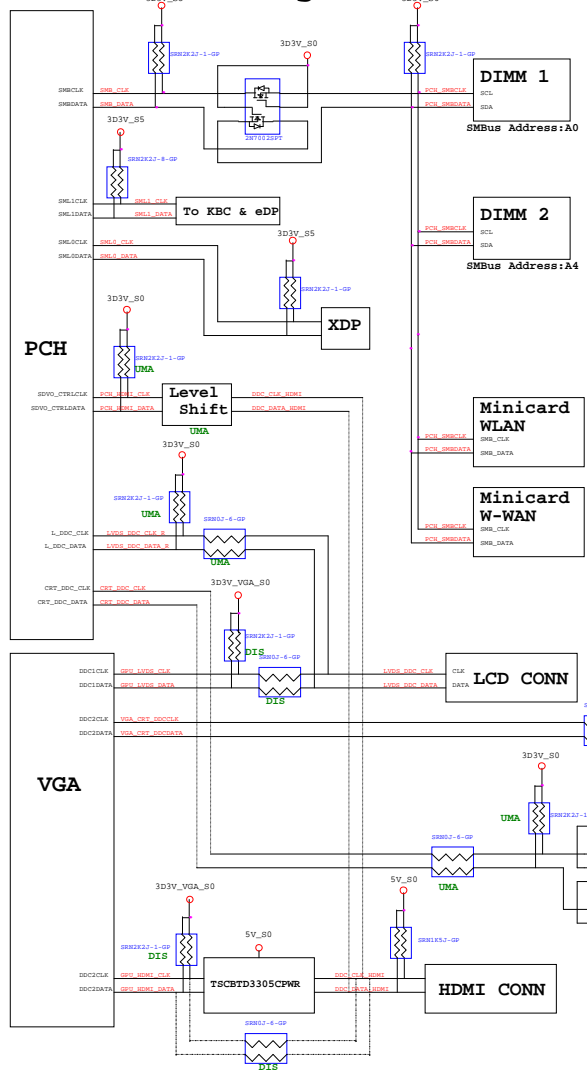
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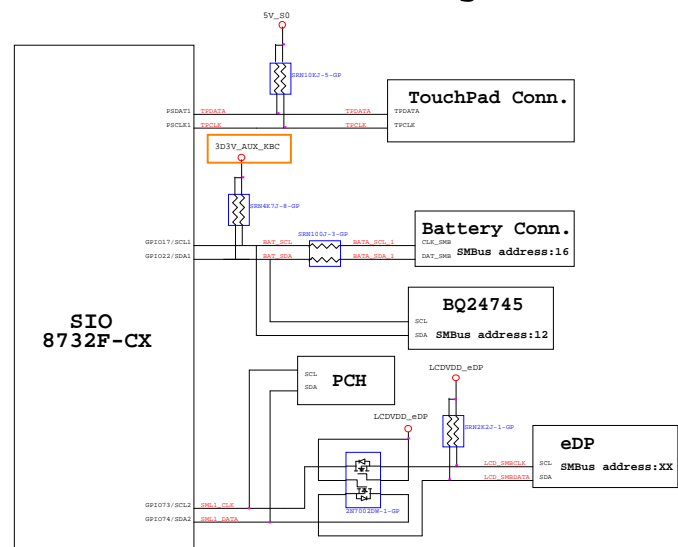
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File	CLOCK MAP		
Size	Document Number	Rev	
C	PIM86L-Florence	1	
Date:	Tuesday, February 25, 2014	Sheet	101 of 103

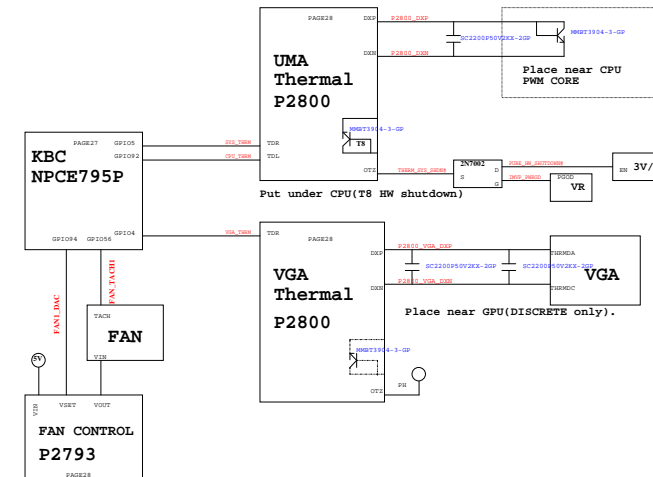
PCH SMBus Block Diagram



SIO SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

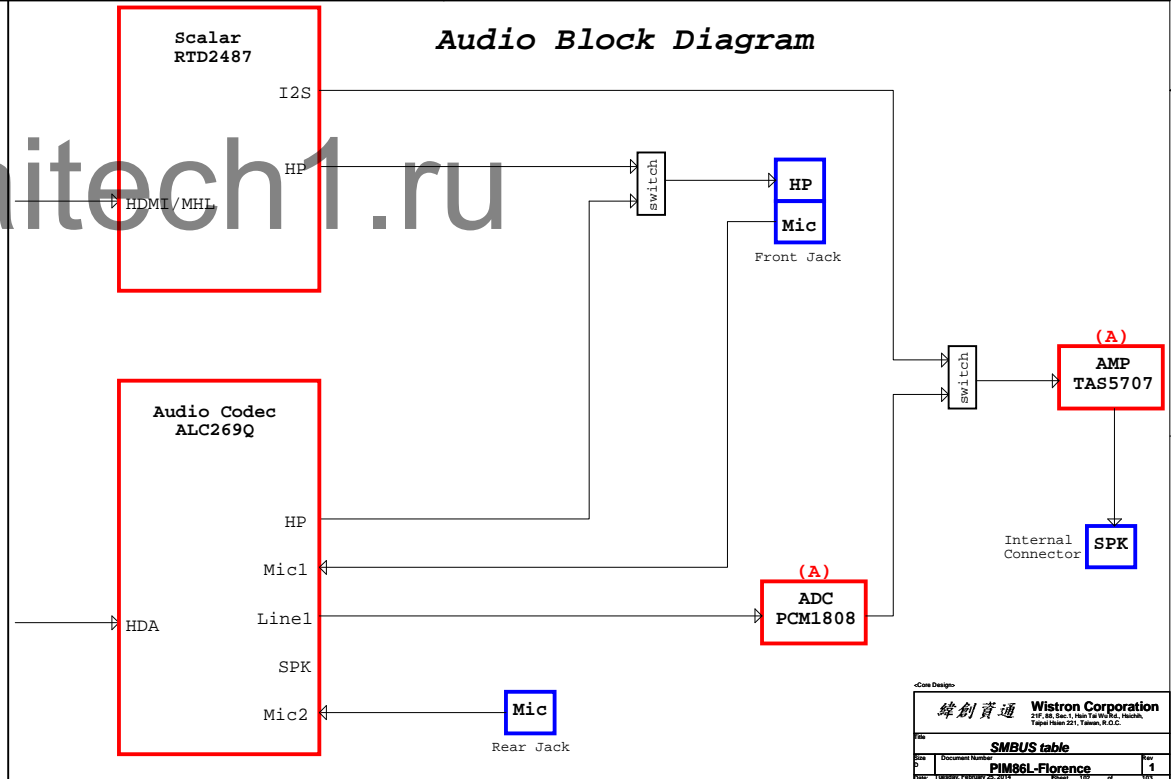
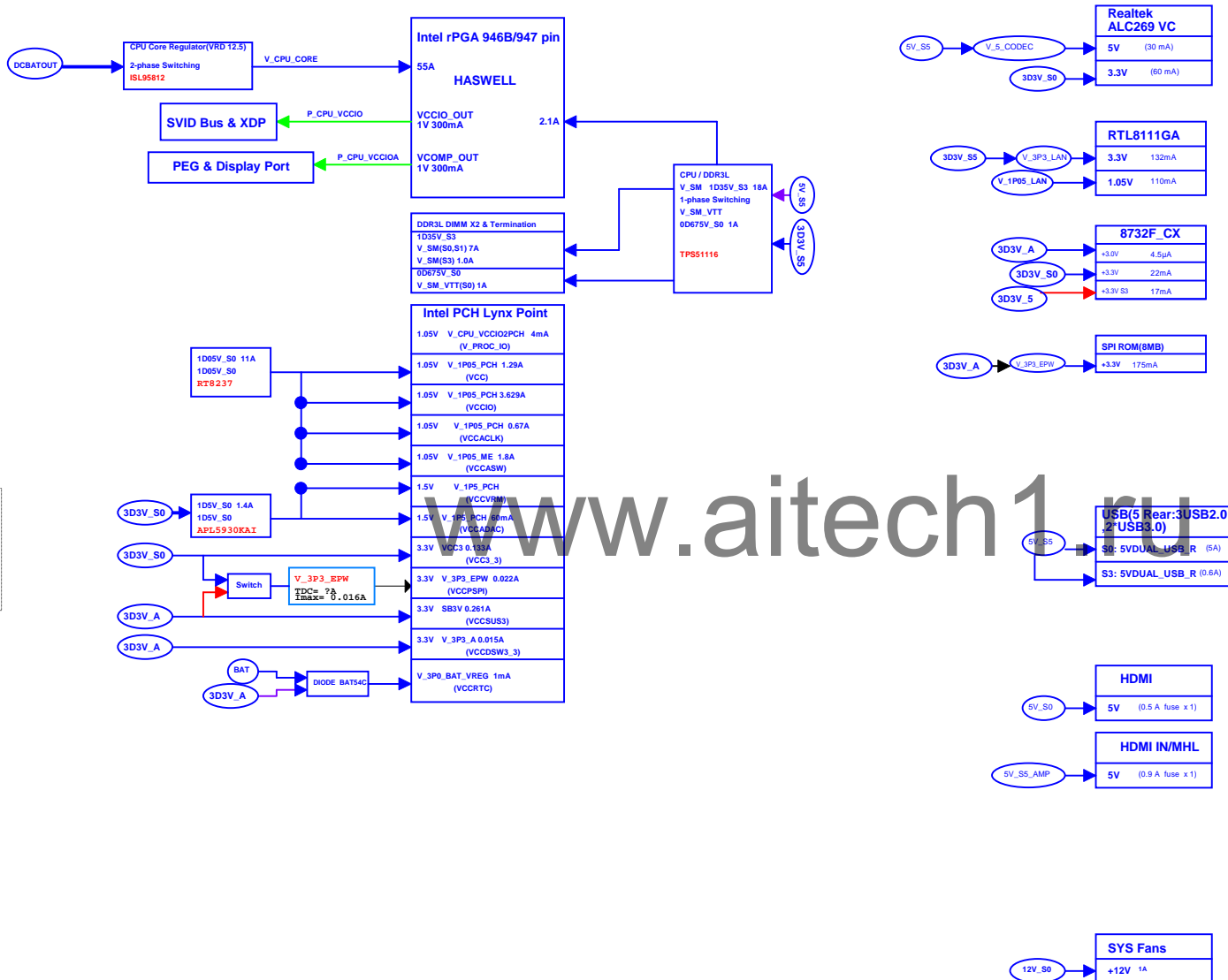


Table 3-3. System with no M3 State Supported.

State	S0/M0	S3/Moff	S4/Moff	S5/Moff	Deep S3	G3*
RTC Well	ON	ON	ON	ON	ON	ON
VCCDSW3_3	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	ON	ON	ON	ON	ON	No Power
V5_0A	ON	ON	ON	ON	OFF	No Power
V3_3A	ON	ON	ON	ON	OFF	No Power
V3_3H	ON	OFF (2)	OFF (2)	OFF (2)	OFF	No Power
V1_1H	ON	OFF	OFF	OFF	OFF	No Power
V1_5U(VDDQ)	ON	ON	OFF	OFF	OFF	No Power
V0_75S	ON	OFF	OFF	OFF	OFF	No Power
V5_0S	ON	OFF	OFF	OFF	OFF	No Power
V3_3S	ON	OFF	OFF	OFF	OFF	No Power
V1_5S	ON	OFF	OFF	OFF	OFF	No Power
V1_0SS	ON	OFF	OFF	OFF	OFF	No Power
V1_0SS_VTT	ON	OFF	OFF	OFF	OFF	No Power
VCCIN	ON	OFF	OFF	OFF	OFF	OFF
VCCST(Ultrabook Only)	ON	OFF	OFF	OFF	OFF	OFF



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